



## Integrated circuits for multimedia applications

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*Publication date:*  
2007

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*Citation (APA):*  
Vandi, L. (2007). *Integrated circuits for multimedia applications*.

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# Integrated circuits for multimedia applications

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*This thesis is submitted in partial fulfillment  
of the requirements for obtaining the Ph.D. degree at:*

Ørsted•DTU  
Technical University of Denmark (DTU)

Kongens Lyngby, 27 September 2006

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ISBN 87-91184-66-5

To Daniela

*She made it possible,  
I just had to get it done.*



# Abstract

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This work presents several key aspects in the design of RF integrated circuits for portable multimedia devices.

One chapter is dedicated to the application of negative-feedback topologies to receiver frontends. A novel feedback technique suitable for common multiplier-based mixers is described, and it is applied to a broad-band dual-loop receiver architecture in order to boost the linearity performances of the stage. A simplified noise- and linearity analysis of the circuit is derived, and a comparison is provided with a more traditional dual-loop topology (a broad-band stage based on shunt-series feedback), showing a difference in compression point in the order of 10dBm for the same power consumption. The same principle is also applied to a more conventional narrow-band stage in which a single loop is employed in order to enhance noise performances. Noise analysis shows sensible improvements in the noise figure (up to  $\sim 1$ dB) in low-performance technologies, when stringent specifications are considered in terms of power consumption.

A recently-reported current-reuse technique, applied to a complete RX frontend, is examined in the following chapter in order to sketch a simplified numerical analysis for the performances of the stage. Semi-ideal models are used in simulations to validate the derived calculations, and the fundamental limits of the basic structure are discussed. The design of a current-mode base-band output stage implemented in a  $0.13\mu\text{m}$  technology is presented: the amplifier draws  $\sim 500\mu\text{A}$  from a 1.2V supply,

providing 35dB gain and 135MHz GBWP.

The integration of high-performance passive components is studied in the last chapter which presents the first reported toroidal inductor fabricated in a standard CMOS process. Field-confinement properties of the structure are exploited in order to reduce the impact of substrate-induced currents. Basic models are derived in the design phase, and the technological limits of the device are considered. Measurement results show that a very compact coil can provide  $\sim 1\text{nH}$  inductance up to 20GHz (physical limit for the measurement equipment), with a peak quality factor around 10 at 15GHz.

# Resumé

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I afhandlingen præsenteres forskellige nøgle-aspekter om design af RF integrerede kredsløb for bærbare multimedia-apparater.

Et kapitel omhandler negativ-feedback topologier til modtager-frontends. En ny feedback-teknik, der passer til almindelige multiplikator-baserede mixere, beskrives og anvendes til en bredbåndsdobbeltsløjfe-modtager-arkitektur for at forbedre trinetts linearitet. En forenklet støj- og linearitetsanalyse af kredsløbet udledes, og en sammenligning gives med en mere traditionel dobbeltsløjfe-konfiguration (et bredbåndstrin baseret på shunt-series feedback), der viser en forskel i kompressionspunktet i nærheden af 10dBm med samme strømforbrug. Det samme princip anvendes til et mere konventionelt smalbåndstrin: en enkeltsløjfe benyttes for at forbedre støjegenskaber. En støjanalyse giver mærkbare forbedringer i støjtal (op til  $\sim 1$ dB) i lavtydende teknologier, når strenge specifikationer med hensyn til strømforbrug tages i betragtning.

En nyligt rapporteret strømgenbrugsteknik (anvendt til en komplet RX-frontend) undersøges i det næste kapitel for at skitsere en simplificeret numerisk analyse af trinetts ydelser. Semi-ideelle modeller bruges i simulationer for at underbygge udledte beregninger, og strukturens grundlæggende grænser klarlægges. Designet af et current-mode base-band udgangstrin realiseret i  $0.13\mu\text{m}$ -teknologi fremvises: forstærkeren trækker  $\sim 500\mu\text{A}$  fra en 1.2V-forsyning og giver 35dB forstærkning sammen med 135MHz GBWP.



Integrationen af højtydende passive komponenter undersøges i det sidste kapitel, der introducerer den første rapporterede toroidal-induktionsspole fabrikeret i standard CMOS teknologi. Strukturens feltsbegrænsningsegenskaber udnyttes for at nedsætte virkningen på substrat-induceret strøm. Grundmodeller udledes i designfasen, og komponentens teknologiske grænser behandles. Måleresultater viser, at en meget kompakt spole kan levere  $\sim 1\text{nH}$  induktans op til 20GHz (fysisk grænse for måleapparatet) med en maksimum kvalitetsfaktor på omkring 10 ved 15GHz.

# Acknowledgements

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“Beggar that I am, I am even poor in thanks;  
but I thank you. [...]”

William Shakespeare, *Hamlet*

This Ph.D. project has been carried out at the Technical University of Denmark (*Danmarks Teknisk Universitet*), and funded by the Danish Research Council for Technology and Production (*Forskningsrådet for Teknologi og Produktion*).

Despite the fact that there is only one name on the front page, this is not a one-man job. I take full responsibility over everything I wrote, but nothing could have been accomplished without help. I’d never be able to mention all the people who have contributed to this work in some way or another, but each of them deserves my complete gratitude.

First of all, I wish to thank my supervisor prof. Pietro Andreani for his constant and vigilant guidance: he has been supporting me all the way through my research period. Thanks to him, I got acquainted with several different people, and I’m grateful to all of them:

- the Ørsted•DTU institute, led by prof. Erik Bruun, which provided a simply perfect working environment for over three years,
- the Microelectronics Lab at University of Pavia (Italy), led by prof. Rinaldo Castello, which welcomed me as a visiting Ph.D. student during my external sojourn,

- the Studium of Microelectronics at ST Microelectronics (Pavia, Italy), an ideal combination of top-class professionalism and helpfulness,
- the R&D group at Ericsson A/B (Lund, Sweden), led by Dr. Carl Fredrik Leanderson, which made me feel, even for a very short time, *part of the team*.

There are a few more people that I'd like to mention specifically, and the reasons are too many to count:

- Allan Jørgensen, with his good mood and extraordinary skills has made many things a huge deal easier,
- Dr. Antonio Liscidini has been an inspiring colleague and a good mate at the same time,
- Dr. Sven Mattisson has always been able to provide the right input at the right time, and his bright ideas have illuminated my path in many occasions.

Finally I wish to thank all the friends that I met since I moved to Denmark: the wonderful memories from the past few years are invaluable.

A handwritten signature in black ink, reading "Luca Vandi". The signature is written in a cursive style, with "Luca" and "Vandi" connected. There is a long, horizontal flourish underneath the name.

Kgs. Lyngby, 27 September 2006

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# List of Symbols and Acronyms

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$2.5D$	Quasi three-dimensional	
$3D$	Three-dimensional	
$AC$	Alternate current	
$ASIC$	Application-specific integrated circuit	
$BW_{-3dB}$	Bandwidth at -3dB	
$C_{gd}$	Gate-drain capacitance of a MOSFET in saturation region	[F]
$C_{gs}$	Gate-source capacitance of a MOSFET in saturation region	[F]
$CMFB$	Common-mode feedback	
$CMOS$	Complementary MOS	
$C'_{ox}$	Field-oxide specific capacitance of a MOS transistor	[F·m <sup>-2</sup> ]
$CP_{1dB,in}$	Input-referred 1dB-compression point . . . . .	[dBm]
$CP_{1dB,out}$	Output-referred 1dB-compression point . . . .	[dBm]
$DC$	Direct current	

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Units are indicated according to the International System (SI), apart from electrical power which is indicated in dBm.

---

$DSB$	Double sideband	
$F$	Noise factor	
$f_{\max}$	Maximum oscillation frequency of a MOS device	[Hz]
$f_{\text{self}}$	Self-resonance frequency of an integrated inductor	[Hz]
$f_T$	Unity-gain frequency of a MOSFET . . . . .	[Hz]
$GBWP$	Gain-bandwidth product . . . . .	[Hz]
$g_{ds}$	Drain-source output conductance of a MOSFET	[A/V]
$G_{loop}$	Closed-loop gain for a feedback system . . . . .	[dB]
$g_m$	Transconductance of a MOSFET . . . . .	[A/V]
$GSG$	Ground-Signal-Ground	
$IC$	Integrated circuit	
$I_D$	Drain current of a MOSFET . . . . .	[A]
$IF$	Intermediate frequency	
$IIP_3$	Input-referred 3 <sup>rd</sup> -order intercept point . . . . .	[dBm]
$\langle i_{n,\text{in}}^2 \rangle$	Input-referred current-noise density . . . . .	[A <sup>2</sup> /Hz]
$j$	Imaginary unit	
$k_B$	Boltzmann constant . . . . .	[J/K]
$L$	Gate length of a MOS transistor . . . . .	[m]
$LC$	Inductor-capacitor	
$L_{\min}$	Minimum gate length of a MOS transistor for a given technology	[m]
$LMV$	LNA-Mixer-VCO	
$LNA$	Low-noise amplifier	
$LO$	Local oscillator	
$MGTR$	Multiple-gated transistors	
$MOS$	Metal-Oxide-Semiconductor	
$MOSFET$	MOS field-oxide transistor	

---

$N_a$	Acceptors' concentration in $pn$ -junctions...	[m <sup>-3</sup> ]
$N_d$	Donors' concentration in $pn$ -junctions.....	[m <sup>-3</sup> ]
$NF$	Noise figure.....	[dB]
$nMOS$	n-channel MOS transistor	
$Op-Amp$	Operational amplifier	
$PAC$	Periodic alternate current	
$pMOS$	p-channel MOS transistor	
$PN$	Phase noise.....	[dBc/Hz]
$PSS$	Periodic steady-state	
$Q$	Quality factor of a resonator	
$q$	Charge of the electron.....	[C]
$RF$	Radio frequency	
$RX$	Receiver	
$s$	Generic complex variable in the Laplace domain	[Hz]
$SC$	Switched capacitors	
$SOI$	Silicon on insulator	
$SOM$	Self-oscillating mixer	
$SSB$	Single sideband	
$T$	Temperature.....	[K]
$t_{ox}$	Gate-oxide thickness.....	[m]
$VCO$	Voltage-controlled oscillator	
$V_{DD}$	Supply voltage of a circuit.....	[V]
$V_{GS}$	Gate-source voltage of a MOSFET.....	[V]
$VLSI$	Very large scale of integration	
$\langle v_{n,in}^2 \rangle$	Input-referred voltage-noise density.....	[V <sup>2</sup> /Hz]
$V_T$	Threshold voltage of a MOS transistor.....	[V]
$W$	Gate width of a MOS transistor.....	[m]
$WLP$	Wafer-level packaging	



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$x_j$	$pn$ -junction depth of MOS systems.....	[m]
$z$	Generic complex variable in the $\mathcal{Z}$ -domain	
$\gamma$	Drain-current thermal noise parameter for MOSFETs	
$\epsilon_{ox}$	Dielectric constant in oxide .....	[F/m]
$\theta$	Vertical-field mobility-reduction parameter of a MOSFET	[V <sup>-1</sup> ]
$\lambda$	Scaling factor for CMOS technology	
$\mu_0$	Magnetic permeability in vacuum .....	[H/m]
$\mu_{n0}$	Nominal carrier mobility for nMOS transistors	[m <sup>2</sup> ·(V·s) <sup>-1</sup> ]
$\phi_m$	Phase-margin of a feedback loop .....	[deg]
$\phi_{th}$	Thermal potential .....	[V]
$\omega_T$	Unity-gain angular frequency of a MOSFET	[rad/s]

## CHAPTER 1

# Introduction

---

“GALLIA EST OMNIS DIVISA IN PARTES TRES [...]”

“All Gaul is divided into three parts [...]”

Caius Iulius Caesar, *Commentarii De Bello Gallico*

Many times since its formulation, *Moore’s Law* [2] has been under discussion, but it proved itself quite impervious to attacks. The main reason behind the exponentially-growing number of components<sup>1</sup> which can be *crammed onto* the same IC is the fact that semiconductor technologies offer devices with smaller and smaller minimum dimensions. Major crisis points have been faced and overcome in multiple occasions, and the improvement rate has been constant [3]; in recent years, the progress of photolithography (among other things) has been so fast that technology enhancements have repeatedly beaten expectations, and forecasts for the near-term future are more optimistic than ever [4], as shown in Figure 1.1. The reduction of minimum dimensions is not enough to explain the astounding progress in VLSI technology: many other parameters have to scale in order to guarantee a reliable development path. It is interesting to notice, though, that

- Moore’s Law had been conceived almost a decade before a proper scaling theory was devised [5], and

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<sup>1</sup>Transistors, in many practical cases.

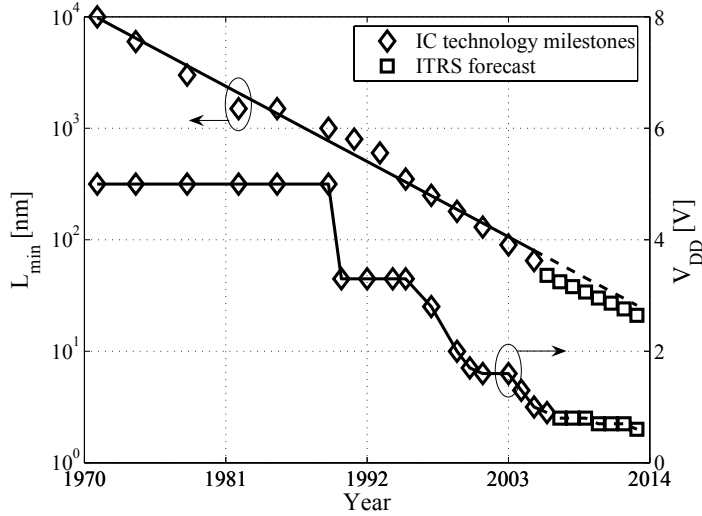


Figure 1.1: Historical data and projections for IC technology development in terms of minimum gate length ( $L_{\min}$ ) and supply voltage ( $V_{DD}$ ). For  $L_{\min}$  a linear fit is indicated for reference.

- the scaling theory itself has not been followed thoroughly, since for example supply voltage has been kept constant for a very long time for no reason but compatibility, as shown in Figure 1.1.

The key-item in scaling theory is the concept of *constant field*, which ensures faster switching of logic gates, lower energy per transition, cheaper devices. In Table 1.1 the main parameters are associated with their respective scaling factor, function of the common factor  $\lambda > 1$ . RF CMOS designers have to face the benefits and the drawbacks of a scaling technique which is targeting purely digital applications.<sup>2</sup> Key aspects like operating frequency, noise and linearity (among others) are heavily influenced by the scaling strategy.

1. Faster logic gates means for certainty higher cut-off frequency  $f_T$  and maximum oscillation frequency  $f_{max}$ , and this has a major positive

<sup>2</sup> “[...] the process is optimized and characterized primarily for one tradeoff: that between speed and power dissipation.” [6]

Table 1.1: Scaling behaviour according to the constant-field theory.

Parameter	Scaling factor
$t_{ox}$	$\frac{1}{\lambda}$
$L$	$\frac{1}{\lambda}$
$W$	$\frac{1}{\lambda}$
$x_j$	$\frac{1}{\lambda}$
$N_a$	$\lambda$
$N_d$	$\lambda$
$V_T$	$\frac{1}{\lambda}$
$V_{DD}$	$\frac{1}{\lambda}$

impact on RF performances [7]. There is also a very peculiar side-effect, though: in inductively-degenerated LNAs the inductance on the source must be inversely proportional to  $f_T$  in order to provide correct input impedance matching, and today designers are finding increasing difficulties in tuning this passive component without sacrificing noise performances.

- Noise performances can be also expected to be positively influenced by scaling, in terms of minimum noise figure as well as sensitivity to deviation from optimal noise matching [8]. Therefore the design of LNAs should be easier, because lower noise levels can be achieved over a wider range of design parameters (bias, transistors' dimensions and so on). It should be noted however that VCO designers will experience serious troubles coping with  $\frac{1}{f}$  noise. Gate-oxide thickness must be scaled together with  $L_{min}$ ; being a few percent of the channel length,  $t_{ox}$  is approaching the sub-nanometre scale, but a thickness below 1nm is not enough to keep direct tunnelling currents at reasonable levels [9]. The introduction of materials with high dielectric constant (so-called "high- $\kappa$  materials") can alleviate this problem, but integration of such structures is still difficult [10], and the poor quality of these insulators leads to bad noise performances [11].
- Linearity is indeed affected by scaling, but in a negative way. It can be shown that optimal biasing for maximum linearity moves toward higher and higher currents [12], and this is in contrast with

the natural tendency to reduce power consumption. The reduction of supply voltage has also a dramatic negative impact on linearity performances.

4. Scaling of threshold voltage has not been very aggressive, and it is probably close to its limits, due to the fact that the value of  $V_T$  is intimately connected to thermal potential  $\phi_{th} = k_B T/q$  [13], therefore apart from reducing operating temperature<sup>3</sup> there are very few chances to overcome this limitation on the long run. Subthreshold operation is widely popular in low-frequency analogue circuits, but it still must be fully exploited in RF, and this is probably one of the main challenges for the incoming years.

The amount of bandwidth *in excess* and the improvement of high-frequency noise performances suggest the possibility to employ negative feedback in order to relax linearity design constraints, particularly in the design of RX front-ends. This goes in the direction of implementing a broadband stage that is capable of handling several communication standards at a time, thereby providing a solution that can serve different applications and is easy to migrate from a technology node to the next, since it relies on non-tuned passives (i.e. resistors) and on transistors' performances that are continuously improving. In Chapter 2 we describe a novel approach to negative feedback applied to Gilbert-cell mixers, that leads to a dual-loop RX front-end with broad-band operation and high linearity. The same principle is also applied to a more traditional single-loop narrow-band stage.

Reduction of supply voltage is simply not enough in order to guarantee a continuous path of lower and lower power consumption, especially considering battery-operated implementations: the number of features increases at a pace hardly sustainable by digital CMOS roadmap. Several design techniques try to address this issue, and current-reusing is definitely one of the most interesting. Recently the first implementation of a stacked structure comprising LNA, mixer and VCO biased by the same current has been proposed [1]. The difficulties of providing the correct trade-offs between all different aspects of RF design just sum up when three different blocks are sharing the same devices (active and passive); the robustness of the design must be thoroughly evaluated, too. In Chapter 3 a simplified analysis is proposed in order to grasp the basic behaviour of the stage and

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<sup>3</sup>This is also a viable option [14], but not for mainstream consumer products.

verify the functionality of the circuit at first order.

The great breakthrough of RF CMOS technology is the possibility of integrating a large amount of digital functions on the same chip together with analogue circuitry, but integration of passive components remains a key necessity in modern radios. Even though we have not examined the subject in detail, we can assume that newer technologies will provide better performances in terms of inductors, varactors and the like [8]. Sharing the same silicon substrate is always a matter of isolating critical parts of the circuit from each other, but this turns out particularly difficult when several coils are integrated on the same die. In the quest for the integration of the *perfect* component (compact, scalable, not prone to inducing currents in the substrate), an implementation of a toroidal inductor is proposed in Chapter 4 in order to demonstrate the superior field-confinement properties of this structure, which has never been implemented in standard CMOS technologies before. Design considerations are presented together with basic modelling and measurement results.

Some conclusions are drawn in the final chapter.



## CHAPTER 2

# Receiver front-ends based on negative feedback

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Traditional active mixers based on the Gilbert cell [15], like the one depicted in Figure 2.1a, are ubiquitous in modern RF architectures. The design of such cells is carried out under the general assumption that the linearity of the block is intimately related to the linearity of the transconductor ( $M_1$  in the figure). To improve linearity performances, several solutions have been devised, most of which are based on the following methods [16]: feedback, feedforward, predistortion and piecewise approximation. In practice many applications exploit a combination of these techniques. A non-exhaustive overview of the most popular approaches includes:

1. source degeneration, which is the most basic form of negative feedback.
2. Stages based on multiple-gated transistors (MGTR) combine opposing nonlinear contributions in order to cancel non-linearities, thereby resembling the feedforward approach [17].
3. Several implementations rely on the MOS I-V characteristic to pre-



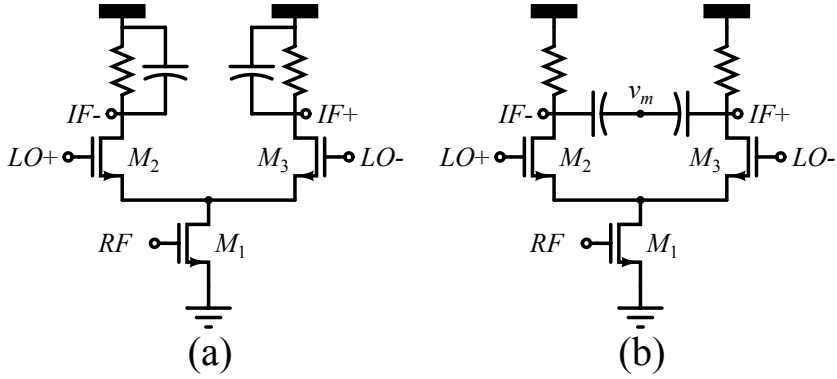


Figure 2.1: A down-conversion mixer based on the Gilbert cell: conventional arrangement (a) and modified topology (b).

distort the input signal and rebuild it at the output, by using for example a transconductor based on a cross-quad cell [16].

4. The so-called CMOS “ $g_m$ -cell”, which is a variant of the bipolar-based “multi-tanh” technique [18] that exploits perfectly the piecewise approximation approach.

In Table 2.1 several solutions found in the literature are presented. Whenever possible, simulation results have been listed, rather than measurement results. Some implementations exploit specific linearization techniques, others are chosen among the present *state-of-the-art*, in order to provide useful comparisons. Feedback-based solutions have been traditionally relegated to low-frequency applications, because of the intrinsic bandwidth reduction associated with the feedback. As more advanced technologies become available, bandwidth limitations become less and less critical. To fully exploit the capabilities of negative feedback, it would be beneficial to embrace the complete cell (transconductor and switching pair) into the feedback loop, rather than closing the loop locally by means of source degeneration.

In Figure 2.1b a slightly-modified multiplier cell is depicted: as explained in the following, the node  $v_m$  offers an unmodulated amplified replica of the input RF signal. This node will be fed back into the loop. The actual implementation of the load might differ, since many different alternatives are feasible, but the basic concept is well illustrated in the figure.

Table 2.1: Reported implementations of down-conversion mixers based on the Gilbert cell.

	Method				Gain	NF	$I_{\text{BIAS}}@V_{\text{DD}}$		$\text{IIP}_3@f_{\text{req.}}$	
	1	2	3	4	[dB]	[dB]	[mA]	[V]	[dBm]	[GHz]
[19]	•				5	18	3.8@2		13@0.9	
[20]	•				9.48	17.69	4.7@2		3@2.4	
[21]	•				10	24.2	0.6@1		6@2	
[22]	•		•		-2.8	N/A	1.4@2.5		-20@N/A	
[23]	•				16	13.1	4@1.8		9@2.1	
[24]				•	26.6	11.9	1.2@1.5		-0.1@2.4	
[25]				•	16.6	16.5	5@1.8		12.12@2.1	
[17]		•			16.5	17.2	3@1.8		9@2.4	
[26]		•			1.7	14.5	4.4@2		4.9@2.4	
[27]		•			-6.5	N/A	3.2@1.25		15@0.9	
[28]			•		3.3	14.87	3.7@1.5		5.46@2.4	
[29]			•		-9.1	N/A	2.5@1.2		9.5@0.9	
[30]		•			6.5	11	6.9@1		3.5@8	
[31]			•		2	13.5	5.2@0.9		3.5@0.9	
[32]		•			4.7	N/A	1.8@1		10.3@5.5	
[33]	•	•			6.6	21.4	N/A@1.8		1.5@1.69	
[34]					6	18.5	7@3.3		11.5@1.9	
[35]					2	N/A	N/A@2		20@24	
[36]					8.3	24.5	5.5@0.9		0@5.25	
[37]					12.76	12.4	1.8@1.8		-6.9@5.7	
[38]					7	N/A	N/A@3.3		4.5@30	
[39]					11.9	13.9	3.2@1		-3@2.4	

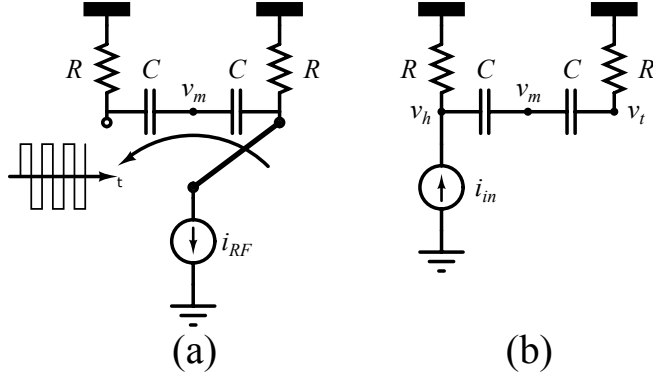


Figure 2.2: Full-switched model of a differential pair used as a mixer (a) and  $R - C$  network resembling the passive load (b).

In Figure 2.2a we have reproduced the cell in Figure 2.1b by modelling the differential pair ( $M_1 - M_2$ ) as a couple of switches, controlled by a time-varying periodic function at frequency  $f_{LO}$ ; we indicate the function as  $m_{LO}(t)$ . The computation of the output voltage can be developed with the aid of Figure 2.2b. We can easily show that the following relations hold:

$$v_h = i_{in} R \frac{1 + s \frac{CR}{2}}{1 + sCR}, \quad (2.1)$$

$$v_t = i_{in} \frac{R}{2} \frac{sCR}{1 + sCR}, \quad (2.2)$$

$$v_m = i_{in} \frac{R}{2}. \quad (2.3)$$

We can then define equivalent impedances, as follows:

$$Z_h \triangleq \frac{v_h}{i_{in}} = R \frac{1 + \frac{sCR}{2}}{1 + sCR}, \quad (2.4)$$

$$Z_t \triangleq \frac{v_t}{i_{in}} = \frac{R}{2} \frac{sCR}{1 + sCR}, \quad (2.5)$$

$$Z_m \triangleq \frac{v_m}{i_{in}} = \frac{R}{2}. \quad (2.6)$$

The application to the structure in Figure 2.2a is straightforward, due to the symmetry properties:

$$\begin{aligned} v_{IF} = & -i_{RF} \frac{1+m_{LO}}{2} Z_h - i_{RF} \frac{1-m_{LO}}{2} Z_t - \\ & - \left( -i_{RF} \frac{1+m_{LO}}{2} Z_t - i_{RF} \frac{1-m_{LO}}{2} Z_h \right). \end{aligned} \quad (2.7)$$

By simplification, we get:

$$\begin{aligned} v_{IF} = & -i_{RF} \cdot m_{LO} (Z_h - Z_t) \\ = & -i_{RF} \cdot m_{LO} \cdot \frac{R}{1+sCR}, \end{aligned} \quad (2.8)$$

which is exactly the result that we expected: the structures in Figure 2.1a and 2.1b are equivalent with respect to the down-converted signal. The fundamental property of middle point  $v_m$  is revealed by the following equation:

$$\begin{aligned} v_m = & -i_{RF} \frac{1+m_{LO}}{2} Z_m - i_{RF} \frac{1-m_{LO}}{2} Z_m \\ = & -i_{RF} \frac{R}{2}. \end{aligned} \quad (2.9)$$

The input RF current is amplified without any kind of filtering nor mixing. This voltage can be used in active feedback circuit topologies, as we will show in the rest of the chapter. More detailed calculations related to the properties of node  $v_m$  can be found in Appendix A.

## 2.1 Dual-loop implementation

Traditional single-stage broad-band LNAs for RF applications present a fundamental trade-off between input matching, noise figure and linearity. The best possible compromise might turn out to be simply not good enough for the particular application. To break the trade-off, several solutions have been proposed, among which feed-forward [40] and negative feedback should be mentioned. The latter is quite popular, but certain limitations occur when a single-loop feedback is implemented. As an example, we can examine the simplified schematic in Figure 2.3. By inspection we can easily get the following result:

$$Z_{in} = \frac{R_f}{1+A}. \quad (2.10)$$

In order to provide correct input matching, the forward gain  $A$  must be carefully controlled. By imposing  $Z_{in} = R_S$  we get:

$$G_{loop} = -\frac{A}{A+2}, \quad (2.11)$$

$$\frac{v_{out}}{v_S} = -\frac{A}{2}. \quad (2.12)$$

The loop gain can not be arbitrarily large, in fact it is going to be smaller than unity. In these conditions, negative feedback does not provide benefits in terms of linearity. For all these reasons, a dual-loop solution is a more sensible choice, but without proper care for the loop properties a dual-loop configuration can not guarantee any benefit by itself. As a practical case, we can study the shunt-series stage depicted in Figure 2.4, which resembles the topology in Figure 2.3 and *does* exhibit a dual loop: the source degeneration ( $R_1$  in the figure) provides a stable forward gain (in principle  $A \approx \frac{R_L}{R_1}$ ) and the shunt feedback (given by  $R_f$ ) defines the correct input matching. However, some limitations occur in practical implementations. We can easily determine the following results:

$$Z_{in} = \frac{(1 + g_{m_1} R_1)(R_f + R_L)}{1 + g_{m_1}(R_1 + R_L)}, \quad (2.13)$$

$$\frac{v_{out}}{v_S} = \frac{Z_{in}}{Z_{in} + R_S} R_L \frac{1 + g_{m_1}(R_1 - R_f)}{(1 + g_{m_1} R_1)(R_f + R_L)}, \quad (2.14)$$

$$G_{loop} = -\frac{g_{m_1} R_L R_S}{(1 + g_{m_1} R_1)(R_f + R_L + R_S)}. \quad (2.15)$$

If we impose perfect matching ( $Z_{in} = R_S$ ), we can determine the value of  $R_f$  as a function of  $R_S$ ,  $R_1$ ,  $R_L$  and  $g_{m_1}$ . By imposing  $R_f > 0$ , we can easily determine a practical limitation for the value of the degeneration resistance:  $R_1 < R_S$ . Since the loop-gain of the series feedback is equal

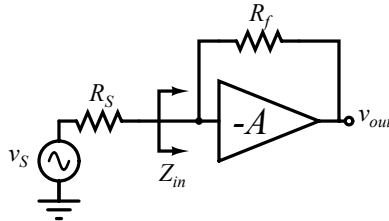


Figure 2.3: A simple negative-feedback stage.

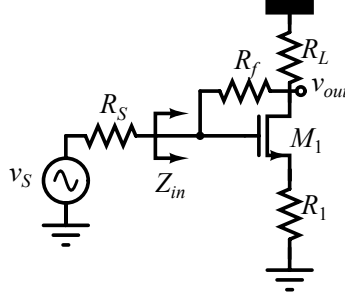


Figure 2.4: A shunt-series input stage.

to  $g_{m_1}R_1$ , given for example  $R_S = 50\Omega > R_1$  it turns out quite difficult to boost such loop-gain way above unity. So the series feedback alone can not provide much benefit in terms of linearization. On the other hand, the same matching condition  $Z_{in} = R_S$  affects  $G_{loop}$  as well, and the expression in (2.15) becomes:

$$G_{loop} = -\frac{g_{m_1}R_L}{g_{m_1}R_L + 2 + 2g_{m_1}R_1}, \quad (2.16)$$

$$|G_{loop}| < 1.$$

We can conclude that any dual-loop topology must provide more degrees of freedom in order to accommodate strict input-matching requirements and highly-demanding linearity specifications.

The proposed topology is shown in Figure 2.5. Both input stage and mixer exhibit local feedback implemented as source degeneration ( $R_{s1}$ ,  $R_2$ ), but the circuit exploits also a dual-loop feedback involving both stages, provided by the node  $v_m$  and the resistor  $R_3$ . Node  $v_m$  can be directly fed back into the loop, since there is no DC coupling. Loads  $R$  and  $R_L$  can be easily implemented by means of active devices, but in the following we will treat them as purely resistive loads. We will show that the dual loop has a high and controllable loop-gain, leading to a robust configuration with good properties in terms of linearity and input matching.

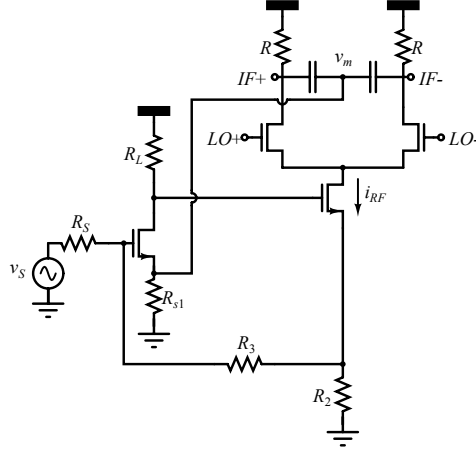


Figure 2.5: A dual-loop high-linearity stage.

### 2.1.1 Circuit analysis

To simplify the analysis of the stage, we consider a stripped-down version operating at a single frequency: as explained in Appendix A, if we neglect the impedance related to capacitance  $C$  we can define an equivalent resistance  $R_1 \triangleq R_{s1} \parallel \frac{R}{2}$  and disregard the mixing operation with respect to RF signals. The simplified schematic is shown in Figure 2.6: the output signal is actually  $i_2$ , which is the RF current that is going to be down-mixed and converted into a differential voltage signal. It might be useful in this case to derive a semi-ideal model based on a single nullor (see Appendix B). The nullor-based schematic is shown in Figure 2.7. Due to the (ideal) properties of the nullor, we easily find:

$$i_2 = \frac{v_a}{R_1}, \quad (2.17)$$

$$i_S = \frac{v_a - R_3 \cdot i_S}{R_2} + i_2, \quad (2.18)$$

from which we can obtain the basic results:

$$Z_{in} = \frac{v_a}{i_S} = \left(1 + \frac{R_3}{R_2}\right) \frac{R_1 R_2}{R_1 + R_2}, \quad (2.19)$$

$$i_2 = v_S \frac{1}{R_1 \left(1 + \frac{R_3}{Z_{in}}\right)}. \quad (2.20)$$

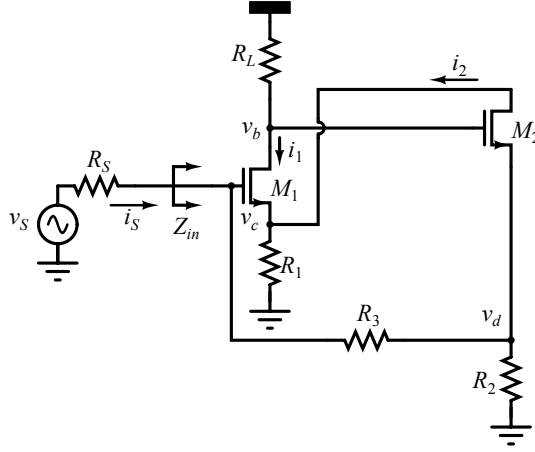


Figure 2.6: Simplified stage for first-order analysis.

Reverting to Figure 2.6, we can derive a proper set of equations:

$$v_a = v_S - R_S i_S, \quad (2.21)$$

$$v_b = -R_L i_1, \quad (2.22)$$

$$v_c = R_1 (i_1 - i_2), \quad (2.23)$$

$$v_d = R_2 (i_S + i_2), \quad (2.24)$$

$$i_S = \frac{v_a - v_d}{R_3}, \quad (2.25)$$

$$i_1 = g_{m1} (v_a - v_c), \quad (2.26)$$

$$i_2 = -g_{m2} (v_b - v_d). \quad (2.27)$$

It is important to notice that these equations, although they do not include but the most ideal parameters, can be easily modified to take parasitics into account, since the number of relevant signals do not change. By solving the equations, we find:

$$R_\Delta \triangleq (R_2 + R_3) \{ (1 + g_{m1} R_1) [1 + g_{m2} (R_2 \parallel R_3)] + g_{m1} g_{m2} R_1 R_L \}, \quad (2.28)$$



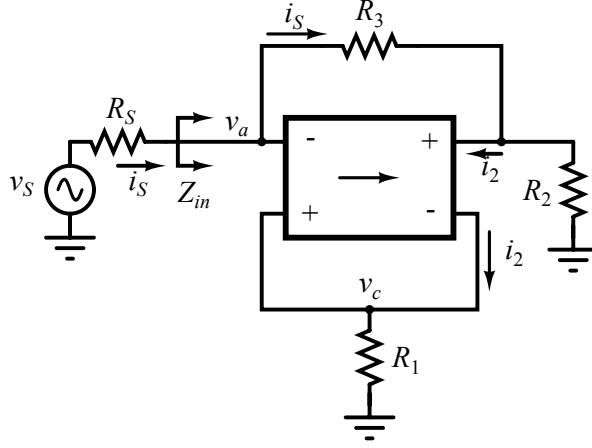


Figure 2.7: Dual-loop stage based on the nullor representation.

$$Z_{in} = \frac{R_{\Delta}}{(1 + g_{m1}R_1)(1 + g_{m2}R_2) + g_{m1}g_{m2}R_L(R_1 + R_2)}, \quad (2.29)$$

$$v_a = v_S \frac{Z_{in}}{Z_{in} + R_S}, \quad (2.30)$$

$$v_b = \frac{-v_a g_{m1} R_L \{R_3 + R_2 [1 + g_{m2}(R_3 - R_1)]\}}{R_{\Delta}}, \quad (2.31)$$

$$v_c = \frac{v_a R_1 \{g_{m2} R_2 + g_{m1}(R_2 + R_3) [1 + g_{m2}(R_L + R_2 // R_3)]\}}{R_{\Delta}}, \quad (2.32)$$

$$v_d = \frac{v_a R_2 \{1 - g_{m1} [g_{m2} R_L (R_3 - R_1) - R_1]\}}{R_{\Delta}}, \quad (2.33)$$

$$i_1 = \frac{v_a g_{m1} [R_2 + R_3 + g_{m2} R_2 (R_3 - R_1)]}{R_{\Delta}}, \quad (2.34)$$

$$i_2 = \frac{g_{m2} v_a \{g_{m1} R_3 R_L + R_2 [1 + g_{m1}(R_1 + R_L)]\}}{R_{\Delta}}. \quad (2.35)$$

Simplifications can be made assuming that  $R_L$  is adequately large, so that  $g_{m1}R_L, g_{m2}R_L \gg 1$ , and  $R_1, R_2 \ll R_L$ . Under these assumptions, we get:

$$Z_{in} \approx \left(1 + \frac{R_3}{R_2}\right) \frac{R_1 R_2}{R_1 + R_2}, \quad (2.36)$$

$$i_2 \approx v_S \frac{1}{R_1 \left(1 + \frac{R_S}{Z_{in}}\right)}, \quad (2.37)$$

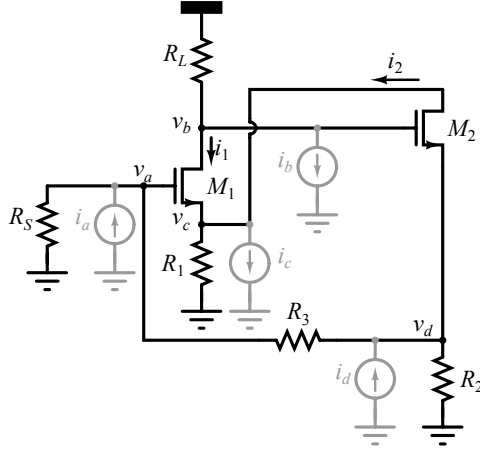


Figure 2.8: Simplified stage for first-order noise calculations.

which can be directly compared with (2.19) and (2.20). Deriving the loop-gain is not obvious, since there are actually two feedback loops. It is anyway easy to notice that by removing the connection from node  $v_b$  to the gate of transistor  $M_2$  we can *cut* the outer loop. The total loop-gain can be determined directly:

$$G_{loop} = -\frac{g_{m1}g_{m2}R_L[R_2R_S + R_1(R_2 + R_3 + R_S)]}{(1 + g_{m1}R_1)\{R_3 + R_S + R_2[1 + g_{m2}(R_3 + R_S)]\}}. \quad (2.38)$$

### 2.1.2 Noise

Some rough noise calculations can be performed with the help of Figure 2.8. It is easy to demonstrate that all relevant noise sources can be seen as linear combination of the currents depicted in the figure, namely  $i_a$ ,  $i_b$ ,  $i_c$  and  $i_d$ . First of all we have to calculate the transfer with respect to these sources:

$$i_2 = G_a \cdot i_a + G_b \cdot i_b + G_c \cdot i_c + G_d \cdot i_d, \quad (2.39)$$

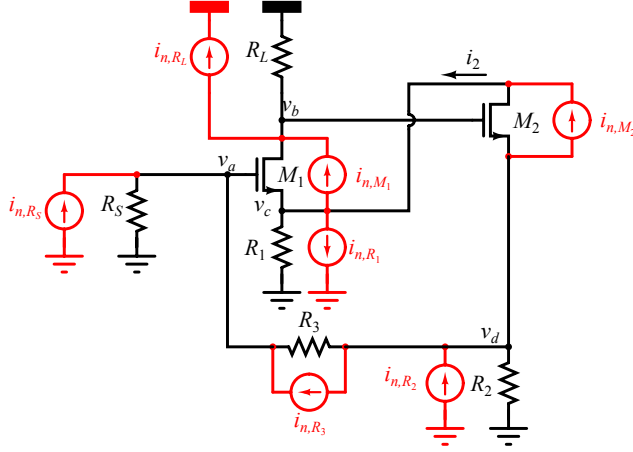


Figure 2.9: Simplified stage with noise sources.

$$G_a = \frac{\frac{R_S Z_{in}}{Z_{in} + R_S} \cdot g_{m2} \{g_{m1} R_3 R_L + R_2 [1 + g_{m1} (R_1 + R_L)]\}}{R_\Delta}, \quad (2.40)$$

$$G_b = \frac{\frac{Z_{in}}{Z_{in} + R_S} \cdot g_{m2} R_L (R_2 + R_3 + R_S) (1 + g_{m1} R_1)}{R_\Delta}, \quad (2.41)$$

$$G_c = \frac{\frac{Z_{in}}{Z_{in} + R_S} \cdot g_{m1} g_{m2} R_1 R_L (R_2 + R_3 + R_S)}{R_\Delta}, \quad (2.42)$$

$$G_d = \frac{\frac{Z_{in}}{Z_{in} + R_S} \cdot g_{m2} R_2 [(R_3 + R_S) (1 + g_{m1} R_1) + g_{m1} R_S R_L]}{R_\Delta}, \quad (2.43)$$

where of course  $R_\Delta$  and  $Z_{in}$  are defined as in (2.28)-(2.29). In Figure 2.9 the main noise sources are depicted. It is then easy to evaluate the different contributions:

$$i_2 = G_a \cdot i_{n,R_S} + G_c \cdot i_{n,R_1} + G_d \cdot i_{n,R_2} + (G_a - G_d) \cdot i_{n,R_3} + (G_c - G_b) \cdot i_{n,M_1} - (G_c + G_d) \cdot i_{n,M_2} + G_b \cdot i_{n,R_L}. \quad (2.44)$$

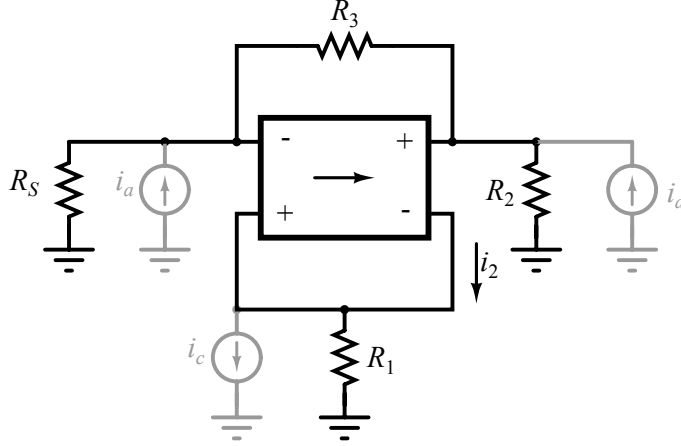


Figure 2.10: Noise analysis of the stage based on the nullor representation.

The noise factor can then be derived directly, considering that all these noise contributions will sum up with the signal:

$$\begin{aligned}
 F = 1 + & \frac{G_c^2 \cdot \overline{i_{n,R_1}^2} + G_d^2 \cdot \overline{i_{n,R_2}^2} + (G_a - G_d)^2 \cdot \overline{i_{n,R_3}^2} + G_b^2 \cdot \overline{i_{n,R_L}^2}}{G_a^2 \cdot \overline{i_{n,R_S}^2}} + \\
 & + \frac{(G_c - G_b)^2 \cdot \overline{i_{n,M_1}^2} + (G_c + G_d)^2 \cdot \overline{i_{n,M_2}^2}}{G_a^2 \cdot \overline{i_{n,R_S}^2}}. \quad (2.45)
 \end{aligned}$$

The above expression can be greatly simplified by means of nullor approximation. First of all, by inspection we find out that node  $v_b$  is actually *inside* the nullor itself. From (2.39) and the following, we derive:

$$\frac{G_b}{G_c} = \frac{1 + g_{m_1} R_1}{g_{m_1} R_1}. \quad (2.46)$$

We can refer to Figure 2.10 to derive new expressions for current gains:

Table 2.2: Different noise contributions in the dual-loop topology.

Source	Contribution
$R_S$	1
$R_1$	$\frac{R_1}{R_S} \left(1 + \frac{R_S}{R_2 + R_3}\right)^2$
$R_2$	$\frac{R_2}{R_S} \left(\frac{R_S}{R_2 + R_3}\right)^2$
$R_3$	$\frac{R_3}{R_S} \left(\frac{R_S}{R_2 + R_3}\right)^2$
$R_L$	$\frac{1}{g_{m1}^2 R_L R_S} \left[ \left(1 + g_{m1} R_1\right) \cdot \left(1 + \frac{R_S}{R_2 + R_3}\right) \right]^2$
$M_1$	$\frac{\gamma}{g_{m1} R_S} \left(1 + \frac{R_S}{R_2 + R_3}\right)^2$
$M_2$	$\gamma \cdot \frac{g_{m2}}{R_S} \left[ \frac{R_1 \cdot (R_2 + R_3 + R_S) + R_S R_2}{R_2 + R_3} \right]^2$

$$G_a \approx \frac{R_S \cdot (R_2 + R_3)}{R_S R_2 + R_1 \cdot (R_2 + R_3 + R_S)}, \quad (2.47)$$

$$G_b \approx \frac{1 + g_{m1} R_1}{g_{m1} R_1} \cdot \frac{R_1 \cdot (R_2 + R_3 + R_S)}{R_S R_2 + R_1 \cdot (R_2 + R_3 + R_S)}, \quad (2.48)$$

$$G_c \approx \frac{R_1 \cdot (R_2 + R_3 + R_S)}{R_S R_2 + R_1 \cdot (R_2 + R_3 + R_S)}, \quad (2.49)$$

$$G_d \approx \frac{R_S R_2}{R_S R_2 + R_1 \cdot (R_2 + R_3 + R_S)}. \quad (2.50)$$

The expression found in (2.45) is still valid. We can write the noise density for a MOS transistor as follows:  $i_{n,M}^2 = 4k_B T \gamma g_m$  (like e.g. in [41], where the typical value of  $\gamma = \frac{2}{3}$  valid for long-channel devices is used). Different contributions are summarized in Table 2.2 (the contribution from the source is unitary). Some useful indications come from this approximated analysis:

- $R_1$  and  $R_3$  should be the dominant noise sources.
- To minimize the overall noise figure,  $R_2$  should be somewhat larger than  $R_1$ , and  $R_1$  should be as small as possible. Reducing  $R_1$  value will eventually lead to:

- a) higher and higher noise contribution from  $M_1$ ,
  - b) lower and lower feed-back loop-gain.
- The limit condition  $R_3 \rightarrow 0$  leads to a theoretical NF > 3dB.

### 2.1.3 Linearity

The linearity analysis can not be performed by *brute force*: introducing arbitrarily non-linear terms in equations (2.21)-(2.27) lead to unmanageable results. A *softer* approach, based on a semi-iterative method, is then preferred. Since our simplified schematic is virtually operating at a single frequency, we want ultimately to derive a polynomial approximation like:

$$i_2 \approx g_S \cdot v_S + \alpha_2 \cdot v_S^2 + \alpha_3 \cdot v_S^3, \quad (2.51)$$

where  $g_s$  is the small-signal transconductance resulting from (2.21)-(2.27), and  $\alpha_2 - \alpha_3$  are appropriate non-linear coefficients. In fact, we will derive only  $\alpha_3$ , since input signal  $v_S$  is a harmonic signal and even-order distortion doesn't affect the transfer properties at the frequency of interest:

$$v_S = v_0 \cdot \cos \omega_0 t, \quad (2.52)$$

$$\begin{aligned} i_2 \approx & \frac{\alpha_2 v_0^2}{2} + \left( g_s v_0 + \frac{3\alpha_3 v_0^3}{4} \right) \cos \omega_0 t + \\ & + \frac{\alpha_2 v_0^2}{2} \cos 2\omega_0 t + \frac{\alpha_3 v_0^3}{4} \cos 3\omega_0 t. \end{aligned} \quad (2.53)$$

The following assumptions are considered:

1. the non-linearities are concentrated on the transconductors, i.e.  $M_1$  and  $M_2$  in Figure 2.6. Equations (2.26)-(2.27) are modified as follows:

$$i_1 = g_{m1}(v_a - v_c) + \widehat{i}_1, \quad (2.54)$$

$$i_2 = -g_{m2}(v_b - v_d) - \widehat{i}_2. \quad (2.55)$$

The new system is solved with respect to non-linear terms  $\widehat{i}_1$  and  $\widehat{i}_2$ :

$$i_2 = g_S \cdot v_S + \widehat{G}_1 \cdot \widehat{i}_1 + \widehat{G}_2 \cdot \widehat{i}_2. \quad (2.56)$$

2. Third-order non-linearities are implemented through empirical factors that depend only on the gate-source voltage:

$$\widehat{i}_1 \triangleq \alpha_{31}(v_a - v_c)^3, \quad (2.57)$$

$$\widehat{i}_2 \triangleq \alpha_{32}(v_b - v_d)^3. \quad (2.58)$$

First we can solve the (still linear) system (2.26)-(2.27) with respect to the non-linear terms defined in (2.54)-(2.55):

$$\widehat{G}_1 = \frac{\frac{Z_{in}}{Z_{in}+R_S} \cdot g_{m2} R_L (R_2 + R_3 + R_S)}{R_\Delta}, \quad (2.59)$$

$$\widehat{G}_2 = -\frac{\frac{Z_{in}}{Z_{in}+R_S} \cdot (1 + g_{m1} R_1)(R_2 + R_3 + R_S)}{R_\Delta}. \quad (2.60)$$

By substitution of (2.57)-(2.58) in (2.56) we find:

$$i_2 = g_S \cdot v_S + \widehat{G}_1 \cdot \alpha_{31}(v_a - v_c)^3 + \widehat{G}_2 \cdot \alpha_{32}(v_b - v_d)^3. \quad (2.61)$$

The expressions of  $v_a$ ,  $v_b$ ,  $v_c$  and  $v_d$  here used are the solutions of the linear system, i.e. (2.30)-(2.33). We introduce those expressions in (2.61) and we radically simplify to get the following result:

$$\begin{aligned} \widehat{R}_T &\triangleq (R_2 + R_3 + R_S) \cdot \left( \frac{Z_{in}}{Z_{in} + R_S} \right)^4, \\ \alpha_3 &= \alpha_{31} \frac{g_{m2} \widehat{R}_T R_L [R_2 + R_3 + g_{m2} R_2 (R_3 - R_1)]^3}{R_\Delta^4} + \\ &\quad + \alpha_{32} \frac{\widehat{R}_T (1 + g_{m1} R_1) \{g_{m2} R_3 R_L + R_2 [1 + g_{m1} (R_1 + R_L)]\}^3}{R_\Delta^4}. \end{aligned} \quad (2.62)$$

To quantify non-linear terms  $\alpha_{31}$  and  $\alpha_{32}$  we have to consider second-order effects in the MOS I-V characteristic: the simple quadratic expression  $I_D \propto (V_{GS} - V_T)^2$  does not provide any high-order non-linearity. Many mechanisms have been studied and implemented in advanced MOS models [42], among which:

- threshold voltage modulation (due to different mechanisms like body effect),

- mobility reduction due to vertical field,
- velocity saturation,
- bulk charge effect.

For the sake of simplicity, only one of them will be examined, and since we have assumed that non-linear terms are functions of the gate-source voltage, mobility reduction due to vertical field is the preferred choice. We rewrite the I-V characteristic as follows:

$$I_D = \frac{1}{2} \frac{\mu_{n0}}{1 + \theta(V_{GS} - V_T)} C'_{ox} \frac{W}{L} (V_{GS} - V_T)^2 \quad (2.64)$$

$$= \frac{k_0}{1 + \theta(V_{GS} - V_T)} (V_{GS} - V_T)^2, \quad (2.65)$$

where

- $\mu_{n0}$  is the effective mobility at  $V_{GS} = V_T$ ,
- $\theta$  is the vertical-field reduction factor and
- $k_0$  is equal to  $\frac{1}{2} \mu_{n0} C'_{ox} \frac{W}{L}$ .

Given an input signal  $v_{gs}$  on top of the bias voltage  $V_{gs}$ , the output current can be determined as a sum of bias current  $I_d$ , a linear term  $i_d$  and a non-linear term  $\hat{i}_d$ :

$$\begin{aligned} I_d + i_d + \hat{i}_d &= \frac{k_0(V_{gs} + v_{gs} - V_T)^2}{1 + \theta(V_{gs} + v_{gs} - V_T)} \\ &= \frac{k_0}{1 + \theta(V_{gs} - V_T)} \frac{(V_{gs} + v_{gs} - V_T)^2}{1 + \frac{\theta v_{gs}}{1 + \theta(V_{gs} - V_T)}}. \end{aligned} \quad (2.66)$$

We can approximate the following term:

$$\frac{1}{1 + \frac{\theta v_{gs}}{1 + \theta(V_{gs} - V_T)}} \approx 1 - \frac{\theta v_{gs}}{1 + \theta(V_{gs} - V_T)}, \quad (2.67)$$



and (2.66) becomes:

$$\begin{aligned}
I_d + i_d + \hat{i}_d &\simeq \frac{k_0(V_{gs} + v_{gs} - V_T)^2}{1 + \theta(V_{gs} - V_T)} \left[ 1 - \frac{\theta v_{gs}}{1 + \theta(V_{gs} - V_T)} \right] \\
&\simeq \frac{k_0(V_{gs} - V_T)^2}{1 + \theta(V_{gs} - V_T)} + \\
&\quad + k_0(V_{gs} - V_T) \frac{2 + \theta(V_{gs} - V_T)}{[1 + \theta(V_{gs} - V_T)]^2} v_{gs} + \\
&\quad + k_0 \frac{1 - \theta(V_{gs} - V_T)}{[1 + \theta(V_{gs} - V_T)]^2} v_{gs}^2 - \\
&\quad - \frac{k_0 \cdot \theta}{[1 + \theta(V_{gs} - V_T)]^2} v_{gs}^3, \tag{2.68}
\end{aligned}$$

$$I_d = \frac{k_0(V_{gs} - V_T)^2}{1 + \theta(V_{gs} - V_T)}, \tag{2.69}$$

$$i_d \simeq k_0(V_{gs} - V_T) \frac{2 + \theta(V_{gs} - V_T)}{[1 + \theta(V_{gs} - V_T)]^2} v_{gs}, \tag{2.70}$$

$$\begin{aligned}
\hat{i}_d &\simeq k_0 \frac{1 - \theta(V_{gs} - V_T)}{[1 + \theta(V_{gs} - V_T)]^2} v_{gs}^2 - \\
&\quad - \frac{k_0 \cdot \theta}{[1 + \theta(V_{gs} - V_T)]^2} v_{gs}^3. \tag{2.71}
\end{aligned}$$

From (2.71) we can derive the third-order polynomial coefficient:

$$\alpha_{3i} \triangleq - \frac{k_{0i} \cdot \theta_i}{[1 + \theta(V_{gs_i} - V_{T_i})]^2}, \tag{2.72}$$

where the index  $i$  refers to the specific transistor  $M_i$ .

### 2.1.4 Numerical results

The simulation of the stage is quite problematic because the different parasitics disseminated in the circuit reduce the loop gain (in magnitude *and* phase) very rapidly. We can identify a few parasitics among the most critical ones:

1. the finite output resistance of the input transistor ( $g_{ds_1}$ ),

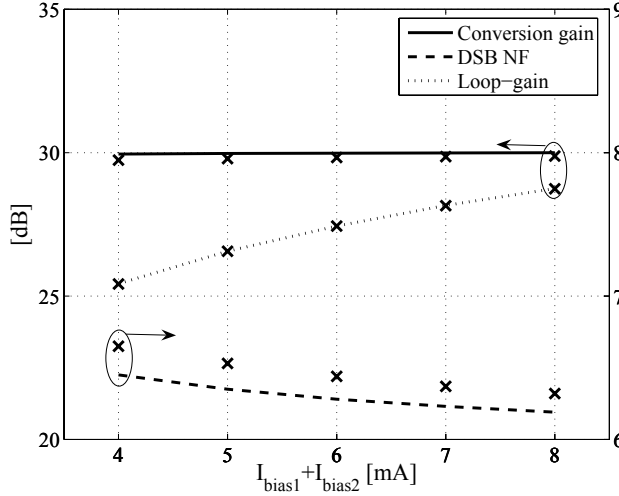


Figure 2.11: Main linear parameters: conversion gain, noise figure and loop-gain. Results from simulations are indicated with “x”-markers.

2. the gate-drain capacitance of the input transistor ( $C_{gd1}$ ),
3. the gate-drain capacitance of the switching pair in the mixer,
4. the total capacitance from the drain of transistor  $M_2$  to ground.

Many solutions can be devised to reduce the effects of these parasitics (for example, an obvious improvement for 1. and 2. would be a cascode transistor), but in this context we want to validate the results derived in the previous sections. Therefore we make use of semi-ideal transistor models, where the main parasitics have been stripped down. These simplifications enable us to perform simulations of critical parameters based on linear analyses (e.g. conversion gain and noise figure), but unfortunately prevent any non-linear simulation from completing successfully. For this reason, non-linear analysis will be entirely based on numerical calculations. Semi-ideal models are based on a  $0.35\mu\text{m}$  process. The bias currents of the input stage ( $I_{bias1}$ ) and the mixer ( $I_{bias2}$ ) are swept at the same time. Calculated values for conversion gain and loop-gain exhibit excellent matching with simulations, whereas NF shows a difference around 0.2dB, due to the fact that the contribution from  $M_2$  at low frequencies has been disregarded.

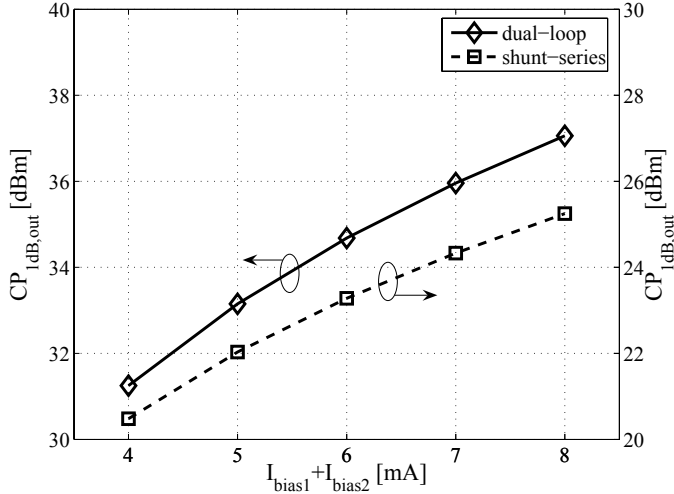


Figure 2.12: Output-referred 1-dB compression point for the proposed circuit and a front-end based on a shunt-series input stage.

Linearity analysis is performed on the basis of the calculations from the previous section. It is useful to have a term of comparison: the same approach that we described in Section 2.1.3 is applied to a front-end based on a shunt-series input stage (see Figure 2.4) and a conventional multiplier-based active mixer (like the one in Figure 2.1). The results are shown in Figure 2.12 in terms of output-referred 1-dB compression point. In Table 2.3 the main design parameters are summarized.

## 2.2 Application to a narrow-band receiver

Narrow-band LNAs based on tuned LC-tanks are extensively used in state-of-the-art receiver chains, where specifications are highly demanding; in Table 2.4 a selection of existing implementations is presented. The selective nature of LC resonators determines a high rejection of adjacent blockers, and the relatively low number of critical noise sources has a positive impact on total noise figure. A simplified configuration is shown in Figure 2.13a: the inductive degeneration provides the correct matching

Table 2.3: Main parameters related to results in Figures 2.11 and 2.12.

	Dual-loop	Shunt-series
$R_S$	$50\Omega$	$50\Omega$
$R_1$	$10\Omega$	$10\Omega$
$R_2$	$10\Omega$	$50\Omega$
$R_3$	$90\Omega$	N/A
$R_f$	N/A	$1\text{k}\Omega$
$R_L$	$3.7\text{k}\Omega$	$3.7\text{k}\Omega$
$R$	$1\text{k}\Omega$	$1\text{k}\Omega$
$I_{bias_1}$	$2\div 4\text{mA}$	$2\div 4\text{mA}$
$I_{bias_2}$	$2\div 4\text{mA}$	$2\div 4\text{mA}$
$V_{DD}$	$2.5\text{V}$	$2.5\text{V}$

[41], and a cascode stage reduces the impact of the Miller effect related to gate-drain capacitance at transistor  $M_1$ . The mixer is built as a direct implementation of the Gilbert multiplier.

The open loop configuration can be easily modified to exploit negative feedback as shown in Figure 2.13b; to simplify the structure the following assumptions are made:

1. The contribution of the cascode transistor in the LNA is omitted.
2. Since we are interested in the operation around resonance, we represent the load LC tank with the equivalent parallel resistance  $R_d$ .
3. No parasitics are considered except for the gate-source capacitance of transistor  $M_1$ . Switches and transconductors are ideal.
4. The quality factor of tuning inductor  $L_g$  is considered infinite.
5. At high frequency, the load resistors of the mixer combine in parallel with the degeneration inductor  $L_s$ . We assume that the equivalent parallel resistance of the inductor is marginally affected.

Table 2.4: Reported implementations of narrow-band receiver front-ends based on tuned LC-tanks.

	Gain [dB]	NF [dB]	Freq. [GHz]	$I_{BIAS}@V_{DD}$ [mA] [V]	Tech. [nm]	
[43]	51.5	2.9	0.894	29@2.6	250	
[44]	7	11.77	1.1	22@1	350	
[45]	28.4	1.4	5	11.2@1.8	180	
[46]	47	5.6	2.1	9@1.8	180	
[47]	92	4.8	1.6	17@1.6	180	<sup>1</sup>
[48]	110	4	1.6	15@1.6	180	<sup>2</sup>
[49]	44	7	1.6	5@1.8	180	
[50]	31	3.5	2.4	3.9@1.8	180	
[51]	17.8	1	2.4	2.3@1.2	180	
[52]	26	3.5	5.825	30@1.2	130	
[53]	30	3	0.915	2@1.8	180	
[54]	28	4.7	2.4	20.3@1.8	180	
<i>ib.</i>	30	5.1	5	25.4@1.8	180	
[55]	28	12.5	60	7.5@1.2	130	<sup>3</sup>
[56]	38	1.8	1.6	60@1.4	90	<sup>4</sup>
[57]	50	3.9	1.9	11@1.2	130	
[58]	20.4	19	2.4	0.5@1	180	<sup>5</sup>
<i>ib.</i>	30.5	10.1	2.4	0.5@1	180	<sup>6</sup>
[59]	33	1.7	0.85	18.6@1.5	65	
[60]	16	8.5	5	6.3@1.8	180	<sup>7</sup>
[61]	31.5	2.1	1.9	22@1.5	90	<sup>8</sup>

- <sup>1</sup> performances refer to the complete radio
- <sup>2</sup> gain and current consumption include the whole chain
- <sup>3</sup> based on common-gate topology
- <sup>4</sup> current consumption refers to the complete radio
- <sup>5</sup> LNA and Mixer are stacked
- <sup>6</sup> folded-cascode LNA+Mixer
- <sup>7</sup> current consumption includes VCO
- <sup>8</sup> current consumption includes LO drivers

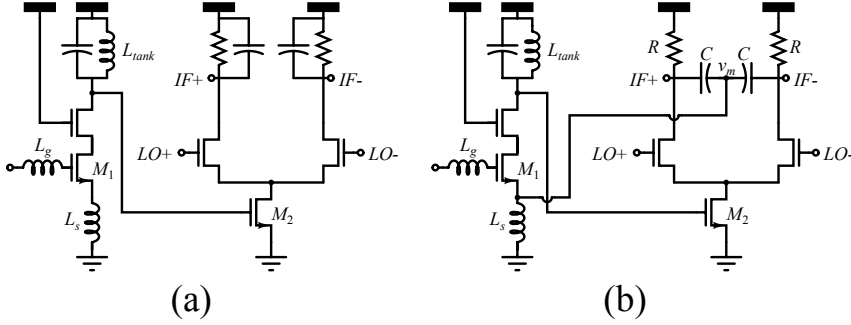


Figure 2.13: A typical LNA-Mixer chain based on LC-tank resonators (a), and the proposed topology (b). Biasing details are omitted.

Concerning the last assumption, we observe that the source-degeneration inductor can be conveniently represented at resonance frequency by an inductance and a series resistance (like in Figure 2.14a) or by an inductance and a parallel resistance (see Figure 2.14b) [16]. The impedance at node  $v_m$  (equal to  $\frac{R}{2} + \frac{1}{s2C}$ ) is connected in parallel, and if we neglect the contribution from capacitance  $2C$  we can define the total impedance as

$$Z_s = sL_p \parallel R_{p1} \parallel \frac{R}{2}. \quad (2.73)$$

According to assumption 5, we consider  $R_{p1} \approx R_{p1} \parallel \frac{R}{2}$ . The simplified circuit results as in Figure 2.15. We will express the degeneration impedance  $Z_s$  in the Laplace domain in the following forms, using well-known series-parallel transformations:

$$Z_s(s) \approx R_1 + sL_s \quad (2.74)$$

$$\approx \frac{sL_p R_{p1}}{R_{p1} + sL_p}. \quad (2.75)$$

### 2.2.1 Circuit analysis

Once again, we study the behaviour of the simplified circuit at a single frequency, and the output signal is the current  $i_2$ . From the figure we can

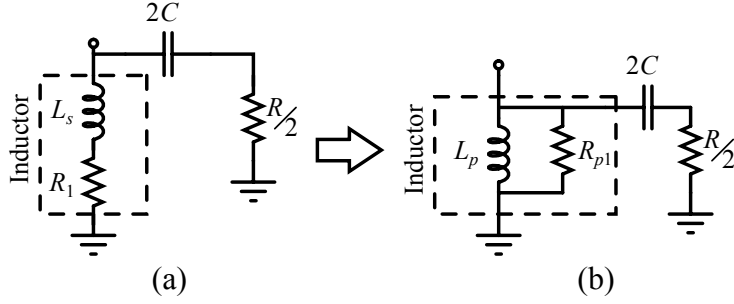


Figure 2.14: Series-parallel transformation of the source-degeneration inductor.

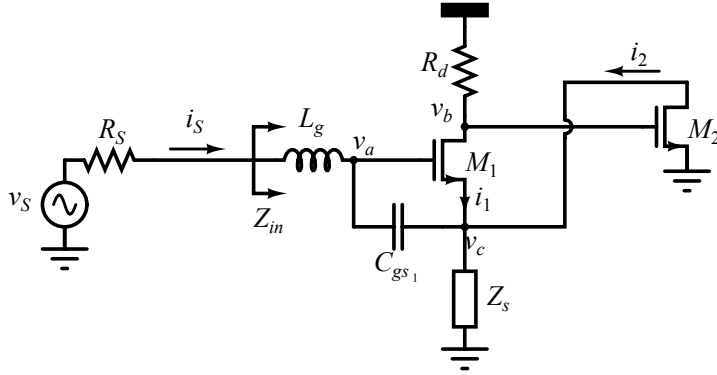


Figure 2.15: Simplified circuit derived from Figure 2.13b.

easily define a fundamental set of equations, like we did for the dual-loop stage:

$$v_a = v_S - i_S(R_S + sL_g), \quad (2.76)$$

$$v_b = -R_d i_1, \quad (2.77)$$

$$v_c = Z_s(s) \cdot (i_S + i_1 + i_2), \quad (2.78)$$

$$i_S = sC_{gs1}(v_a - v_c), \quad (2.79)$$

$$i_1 = g_{m1}(v_a - v_c), \quad (2.80)$$

$$i_2 = -g_{m1}v_b. \quad (2.81)$$

First of all, we can easily determine the input impedance as follows:

$$Z_{in}(s) = \frac{1}{sC_{gs1}} + sL_g + Z_s(s) + \frac{g_{m1}Z_s(s)}{sC_{gs1}}(1 + g_{m2}R_d). \quad (2.82)$$

The result does not differ from the usual one [41] except for the multiplying factor  $(1 + g_{m2}R_d)$ . By using (2.74) we find:

$$Z_{in}(s) = R_1 + \frac{g_{m1}L_s}{C_{gs1}}(1 + g_{m2}R_d) + s \cdot (L_g + L_s) + \frac{1 + g_{m1}R_1(1 + g_{m2}R_d)}{sC_{gs1}}. \quad (2.83)$$

We define the unity-gain frequency  $\omega_T \triangleq \frac{g_{m1}}{C_{gs1}} = 2\pi f_T$  for transistor  $M_1$ , and we can determine the degeneration inductance  $L_s$  and the tuning inductance  $L_g$  by imposing input matching at the operating frequency  $\omega_0$ :

$$\Re[Z_{in}(j\omega_0)] = R_S \Rightarrow L_s = \frac{R_S - R_1}{\omega_T(1 + g_{m2}R_d)}, \quad (2.84)$$

$$\Im[Z_{in}(j\omega_0)] = 0 \Rightarrow L_g = \frac{1 + g_{m1}R_1(1 + g_{m2}R_d)}{\omega_0^2 C_{gs1}} - L_s. \quad (2.85)$$

The optimal value for  $L_s$  will be effectively smaller, compared to the traditional open-loop case, by a factor equal to  $(1 + g_{m2}R_d)$ ; this can be a significant problem in high-performance technologies, since the low value of  $L_s$  can be difficult to control accurately. The tuning inductance  $L_g$  will not differ substantially, since  $g_{m1}R_1 \ll 1$ . We can determine the transconductance of the stage as follows:

$$g_s \triangleq \frac{i_2}{v_S}, \quad (2.86)$$

$$g_s(s) = \frac{g_{m1}g_{m2}R_d \frac{Z_{in}(s)}{Z_{in}(s) + R_S}}{1 + s \cdot C_{gs1}[s \cdot L_g + Z_s(s)] + g_{m1}Z_s(s)(1 + g_{m2}R_d)}. \quad (2.87)$$

The expression in (2.87) can be greatly simplified if we assume perfect matching at the resonance frequency:

$$g_s(s) = \frac{1}{2} \frac{g_{m1}g_{m2}R_d}{s \cdot C_{gs1}R_S}, \quad (2.88)$$

which is the same result that we would obtain with an open-loop stage. Therefore the total conversion gain is not affected by the feedback.

From equations (2.76)-(2.81) we can derive an expression for the loop-gain. By using the same technique described at the end of Section 2.1.1 we find:

$$G_{loop}(s) = -\frac{g_{m1}g_{m2}R_dZ_s(s)}{1 + g_{m1}Z_s(s) + s \cdot C_{gs1}[R_S + s \cdot L_g + Z_s(s)]}. \quad (2.89)$$



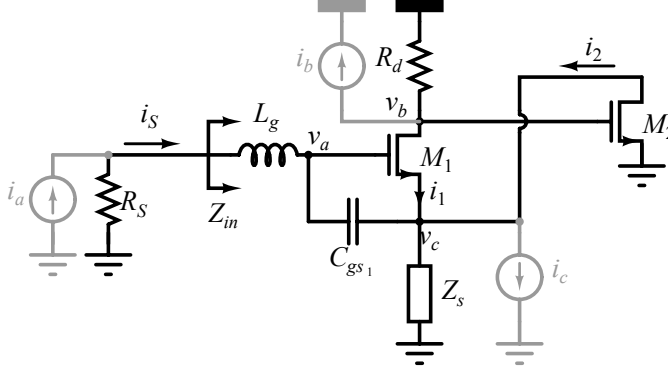


Figure 2.16: Simplified stage for first-order noise calculations.

To simplify the expression we might try to evaluate the limit for  $R_1 \rightarrow 0$ :

$$\lim_{R_1 \rightarrow 0} G_{loop}(j\omega_0) = -\frac{g_{m2}R_d}{2 + g_{m2}R_d}, \quad (2.90)$$

which shows that the loop-gain is smaller than unity in magnitude around the operating frequency.

## 2.2.2 Noise

Noise analysis is performed by means of fictitious current sources  $i_a$ ,  $i_b$  and  $i_c$  shown in Figure 2.16, like in Section 2.1.2. The transfer functions are easily determined:

$$i_2 = G_a \cdot i_a + G_b \cdot i_b + G_c \cdot i_c, \quad (2.91)$$

$$G_a(s) = \frac{g_{m1}g_{m2}R_dR_S}{1 + sC_{gs1}[sL_g + Z_s(s)] + g_{m1}Z_s(s)(1 + g_{m2}R_d)}, \quad (2.92)$$

$$G_b(s) = \frac{g_{m2}R_d\{1 + g_{m1}Z_s(s) + sC_{gs1}[sL_g + R_S + Z_s(s)]\}}{1 + sC_{gs1}[sL_g + R_S + Z_s(s)] + g_{m1}Z_s(s)(1 + g_{m2}R_d)}, \quad (2.93)$$

$$G_c(s) = \frac{g_{m1}g_{m2}R_dZ_s(s)}{1 + sC_{gs1}[sL_g + R_S + Z_s(s)] + g_{m1}Z_s(s)(1 + g_{m2}R_d)}. \quad (2.94)$$

In this simplified analysis, induced gate noise is neglected: even though it plays an important role in inductively-degenerated LNAs [62], its contribution will be the same for both structures in Figure 2.13. In Figure 2.17

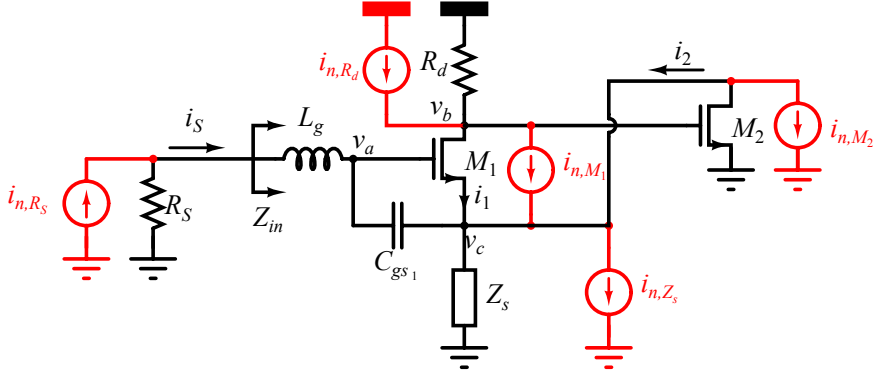


Figure 2.17: Simplified stage with noise sources.

the main noise sources are depicted. The different contributions around operating frequency are evaluated as follows:

$$\begin{aligned}
 F &= 1 + \frac{\overline{i_{n,M_1}^2} \cdot |G_c(j\omega_0) - G_b(j\omega_0)|^2 + \overline{i_{n,M_2}^2} \cdot |G_c(j\omega_0)|^2}{\overline{i_{n,R_S}^2} \cdot |G_a(j\omega_0)|^2} + \\
 &\quad + \frac{\overline{i_{n,Z_s}^2} \cdot |G_c(j\omega_0)|^2 + \overline{i_{n,R_d}^2} \cdot |G_b(j\omega_0)|^2}{\overline{i_{n,R_S}^2} \cdot |G_a(j\omega_0)|^2} \\
 &= 1 + \gamma g_{m1} R_S \left| \frac{G_c(j\omega_0) - G_b(j\omega_0)}{G_a(j\omega_0)} \right|^2 + \gamma g_{m2} R_S \left| \frac{G_c(j\omega_0)}{G_a(j\omega_0)} \right|^2 + \\
 &\quad + \frac{R_S}{R_{p1}} \left| \frac{G_c(j\omega_0)}{G_a(j\omega_0)} \right|^2 + \frac{R_S}{R_d} \left| \frac{G_b(j\omega_0)}{G_a(j\omega_0)} \right|^2. \quad (2.95)
 \end{aligned}$$

To provide a useful comparison with the traditional open-loop stage, we summarize the different contributions to the total noise factor in Table 2.5. The results are calculated around operating frequency for  $R_1 \rightarrow 0$ . The factor related to  $M_2$  includes two terms, because the transistor generates noise at high frequency (and it gets down-converted together with the signal) and at low frequency (where  $\frac{1}{f}$ -noise will be dominant, even though we have chosen not to include it explicitly in the calculations); the simplified formula overestimates the latter term quite a bit. In the closed-loop solution several terms exhibit improvements in noise contributions, specifically  $M_2$ ,  $R_d$  and  $R_{p1}$ .

Table 2.5: Noise contributions for the proposed stage compared to the traditional case.

	Closed loop	Open loop
$R_S$	1	1
$M_1$	$\gamma g_{m_1} R_S \left( \frac{\omega_0}{\omega_T} \right)^2$	$\gamma g_{m_1} R_S \left( \frac{\omega_0}{\omega_T} \right)^2$
$M_2$	$\gamma g_{m_2} R_S \left( \frac{\omega_0}{\omega_T} \right)^2 \frac{1}{(1+g_{m_2} R_d)^2} +$ $+ \gamma g_{m_2} R_S \left( \frac{\omega_0}{\omega_T} \right)^2 \frac{1}{2} \left( \frac{\pi}{g_{m_2} R_d} \right)^2$	$\gamma g_{m_2} R_S \left( \frac{\omega_0}{\omega_T} \frac{1}{g_{m_2} R_d} \right)^2 \left( 4 + \frac{\pi^2}{2} \right)$
$R_{p1}$	$\frac{R_S}{R_{p1}} \left( \frac{\omega_0}{\omega_T} \frac{1}{1+g_{m_2} R_d} \right)^2$	$\frac{R_S}{R_{p1}} \left( \frac{\omega_0}{\omega_T} \right)^2$
$R_d$	$\frac{R_S}{R_d} \left( \frac{\omega_0}{\omega_T} \frac{2+g_{m_2} R_d}{1+g_{m_2} R_d} \right)^2$	$\frac{R_S}{R_d} \left( 2 \frac{\omega_0}{\omega_T} \right)^2$
$R$	$\frac{R_S}{R} \left( \frac{\omega_0}{\omega_T} \frac{\pi}{g_{m_2} R_d} \right)^2$	$\frac{R_S}{R} \left( \frac{\omega_0}{\omega_T} \frac{\pi}{g_{m_2} R_d} \right)^2$

### 2.2.3 Numerical analysis

Like we did in Section 2.1.4, we use simplified models to perform simulations. In this case, only linear parameters will be extracted, so we can compare simulations results with previously derived calculations. From a quick glance at Table 2.5 we can conclude that the most critical parameters in noise analysis are the unity-gain frequency  $f_T$  and the transconductance of the second stage  $g_{m_2}$ ; therefore sweeping the bias current of the second stage ( $I_{bias_2}$ ) and the unity-gain frequency sounds like a sensible choice. Figure 2.18 shows that the noise contribution from transistor  $M_2$  is actually overestimated, but the general trend of the calculations match the behaviour seen in simulations. The difference between open-loop and closed-loop solution can be as high as  $\sim 0.76$ dB. Simulations are based on a  $0.35\mu\text{m}$  process, and the main parameters are summarized in Table 2.6.

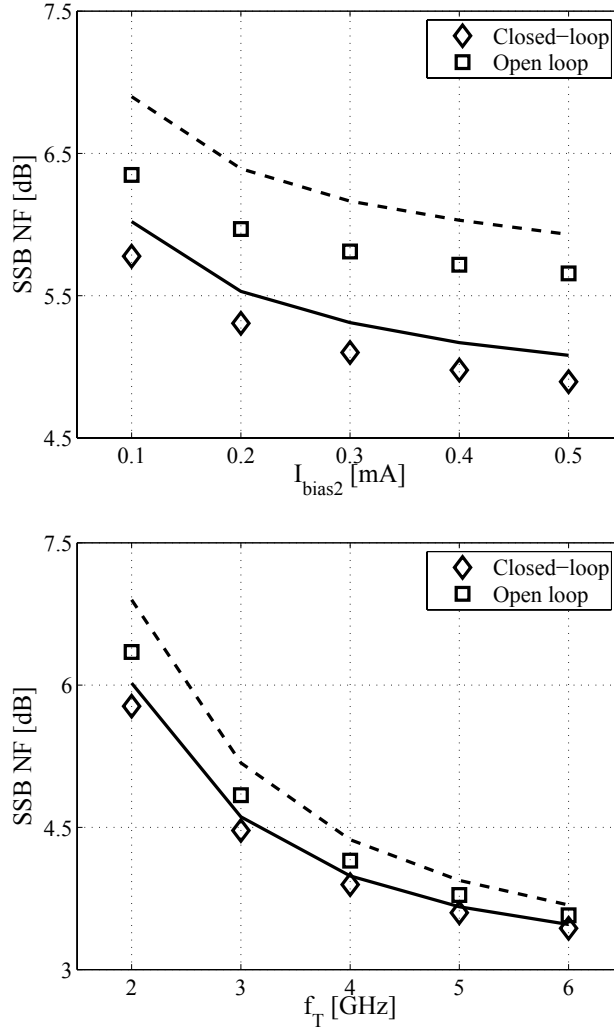


Figure 2.18: Noise figure as a function of mixer bias current (top) and unity-gain frequency (bottom) for the proposed stage and the traditional open-loop stage. Calculations are shown as lines (continuous line and dashed line respectively), whereas simulations are indicated with markers.

Table 2.6: Main parameters related to results in Figure 2.18.

	Closed loop	Open loop	
$R_S$	$50\Omega$	$50\Omega$	
$I_{bias_1}$	2mA	2mA	
$I_{bias_2}$	0.1-0.5mA	0.1-0.5mA	<sup>1</sup>
	0.1mA	0.1mA	<sup>2</sup>
$f_T$	2GHz	2GHz	<sup>1</sup>
	2-6GHz	2-6GHz	<sup>2</sup>
$V_{DD}$	2.5V	2.5V	
$f_{LO}$	900MHz	900MHz	
$Q@f_{LO}$	10	10	
$L_{tank}$	2nH	2nH	

<sup>1</sup> conditions for results in Figure 2.18 (top)<sup>2</sup> conditions for results in Figure 2.18 (bottom)

## CHAPTER 3

# Simplified analysis of a current-reuse LNA-Mixer-VCO architecture

---

In the past years, battery-operated portable devices have been pushing the development of power-saving techniques to the limit. Approaches based on current reuse are extremely effective, for different reasons:

- the supply voltage of large systems is determined by complex architecture specifications, if not by the voltage provided by the battery itself. Therefore even if a single block *could* be operated at a much lower voltage, in practice this is not a viable option to save power.
- Given a certain supply voltage, current consumption of different blocks is determined by a number of non-trivial trade-offs, but it is generally possible to identify one or very few *critical* blocks that determine a lower bound for power usage.

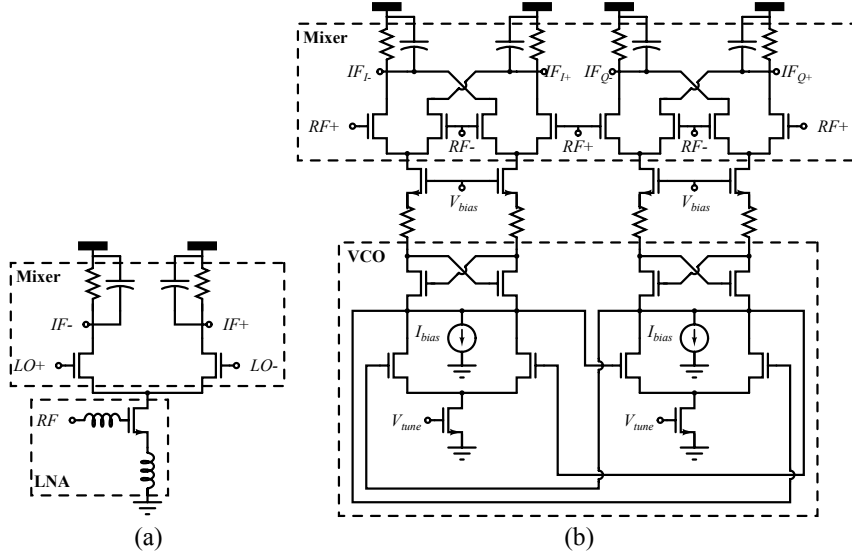


Figure 3.1: Examples of current-reuse topologies: a stacked LNA-Mixer (a) and a self-oscillating mixer (b).

To get as close as possible to the aforementioned lower limit, stacking multiple stages over the same bias source sounds like a very sensible choice. A couple of popular examples are given in Figure 3.1:

- (a) a narrow-band LC-based LNA can provide bias current for a conventional Gilbert-based mixer [63][64],
- (b) the bias current of a VCO can be used to supply a common-base double-balanced mixer [65]. These architectures are commonly referred to as self-oscillating mixers (SOM).

The LNA-Mixer-VCO (LMV) architecture presented in [1] is capable of stacking an LNA, a mixer and a VCO over the same bias current. LC-tank VCOs and active mixers share the same principle (i.e. a pair of switching MOS transistors), but the LC-tank can not offer high impedance at low frequencies (where the down-converted signal should be collected): an additional stage must be inserted, thereby providing isolation between the LO output and the down-converted signal. A schematic of the LMV

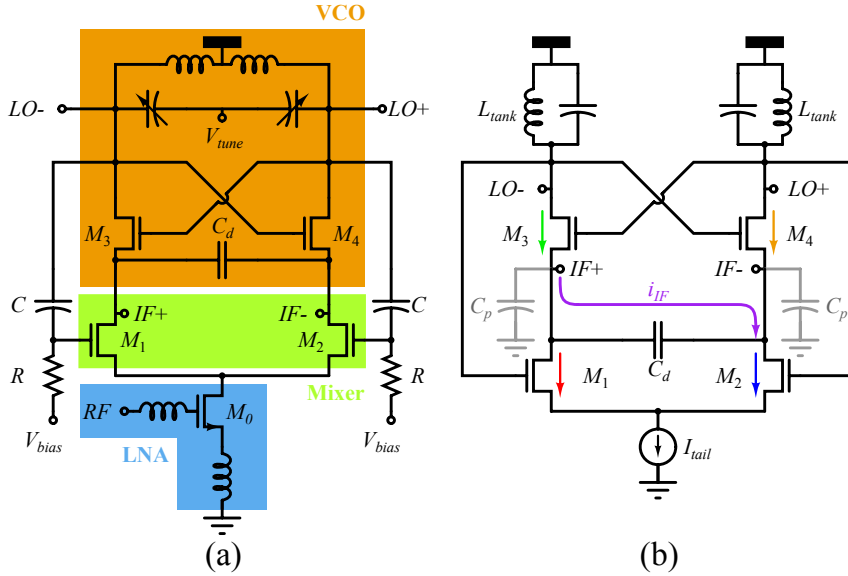


Figure 3.2: The LMV cell: complete circuit (a) and simplified schematic with parasitics at output nodes (b).

cell is reproduced in Figure 3.2a:

- transistor  $M_0$  is a transconductor configured as a narrow-band LNA, which is also supplying bias current for the rest of the circuit.
- Transistors  $M_3 - M_4$  provide the necessary negative resistance to induce oscillation; capacitor  $C_d$  should behave as a short-circuit at radio frequencies.
- Transistors  $M_1 - M_2$  are operated as switches to synthesize the mixing function. The  $R - C$  network is just a decoupling high-pass filter that carries the LO signal back to the input of the mixer.

The adopted description is very simplified and somehow inaccurate (e.g. we can say that  $M_3 - M_4$  are also involved in the mixing operation), but it can be useful to a large extent for a first-order analysis of the stage. Calculating the transfer characteristic of this cell (i.e. the conversion gain and the output bandwidth, among other things) is not obvious, since there



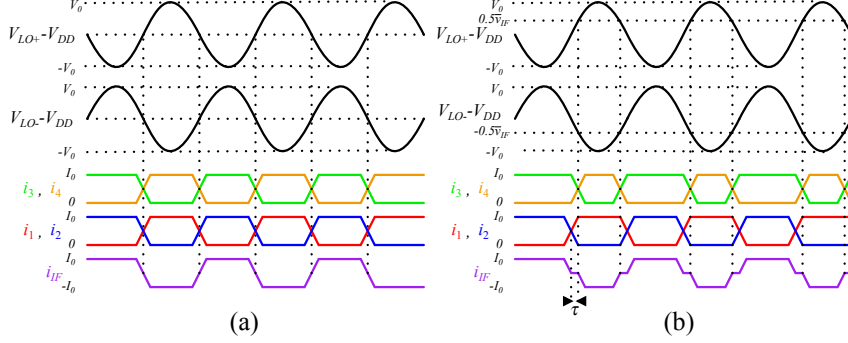


Figure 3.3: Waveforms for the simplified schematic in Figure 3.2b: steady-state operation for  $v_{IF} = 0$  (a) and perturbed waveforms when a signal  $v_{IF}$  is applied (b).

is apparently no load to convert the IF current signal into a differential voltage (like the  $R - C$  low-pass filter in Figure 3.1a, for instance). In particular, the influence of parasitics at the output nodes must be taken in serious consideration. Based on the simplified schematic in Figure 3.2b, we will develop a first-order analysis of the stage, in order to quantify the impact of parasitic capacitance  $C_p$ . As a fundamental precondition, we assume that transistors  $M_1 - M_4$  behave as ideal switches.

### 3.1 Effective resistance at output nodes

First of all, we consider the limit case  $C_p \rightarrow 0$ . Referring to Figure 3.2b, we define:

$$I_{tail} = I_0 + i_{RF} \cdot \sin(\omega_{RF}t), \quad (3.1)$$

$$V_{LO+} = V_{DD} + V_0 \cdot \sin(\omega_0t), \quad (3.2)$$

$$V_{LO-} = V_{DD} - V_0 \cdot \sin(\omega_0t). \quad (3.3)$$

For  $i_{RF} = 0$ , transistors  $M_1 - M_4$  are switching on and off periodically, and we can easily conclude that the couple  $M_1, M_4$  is on half of the time, whereas the couple  $M_2, M_3$  is on the rest of the time. All relevant waveforms are summarized in Figure 3.3a. We will show that by applying a

probe signal  $v_{IF} = v_{IF+} - v_{IF-}$  at low frequency and evaluating the current  $i_{IF}$  associated with it, we can calculate an equivalent resistance  $R_{IF}$ .

We assume that the test signal does not interfere with the oscillation, therefore waveforms  $V_{LO+}$  and  $V_{LO-}$  do not change. We can also safely assume that the behaviour of the couple  $M_1, M_2$  is not affected at the first order, since a low-frequency voltage at the drains does not influence normal operation; finally, we observe that the couple  $M_3, M_4$  will *indeed* be affected, since one transistor will be on for a longer time and the other will be on for a shorter time: the reason is related to the fact that the switching threshold is reduced for one transistor and increased for the other. The concept is illustrated by the waveforms in Figure 3.3b: in every half-period, there is a time-slot  $\tau$  in which the tail current  $I_0$  is flowing entirely either through  $M_1, M_3$  or through  $M_2, M_4$ . We can easily derive the following equations:

$$\frac{\overline{v_{IF}}}{2} = V_0 \sin \omega_0 \tau, \quad (3.4)$$

$$\overline{i_{IF}} = \frac{I_0 \frac{T_0}{2} - I_0 \left( \frac{T_0}{2} - 2\tau \right)}{T_0}, \quad (3.5)$$

where  $T_0 = \frac{2\pi}{\omega_0}$ . From the previous equations, we can determine

$$\begin{aligned} \tau &= \frac{1}{\omega_0} \arcsin \frac{\overline{v_{IF}}}{2V_0} \\ &\approx \frac{\overline{v_{IF}}}{2\omega_0 V_0}, \end{aligned} \quad (3.6)$$

$$\begin{aligned} \overline{i_{IF}} &= \frac{2I_0 \tau}{T_0} \\ &\approx \frac{\overline{v_{IF}}}{2\omega_0 V_0} \frac{2I_0}{T_0} = \frac{I_0}{2\pi V_0} \overline{v_{IF}}, \end{aligned} \quad (3.7)$$

$$\begin{aligned} R_{IF} &\triangleq \frac{\overline{v_{IF}}}{\overline{i_{IF}}} \\ &\approx \frac{2\pi V_0}{I_0}. \end{aligned} \quad (3.8)$$

The last equation shows that there is an *effective* resistance acting at low frequencies, which is related to the amplitude of the oscillation and to the bias current. We can also express (3.8) in another form:

$$\frac{V_0}{I_0} \approx \frac{1}{\pi} \omega_0 L_{tank} Q \implies R_{IF} \approx 2\omega_0 L_{tank} Q, \quad (3.9)$$

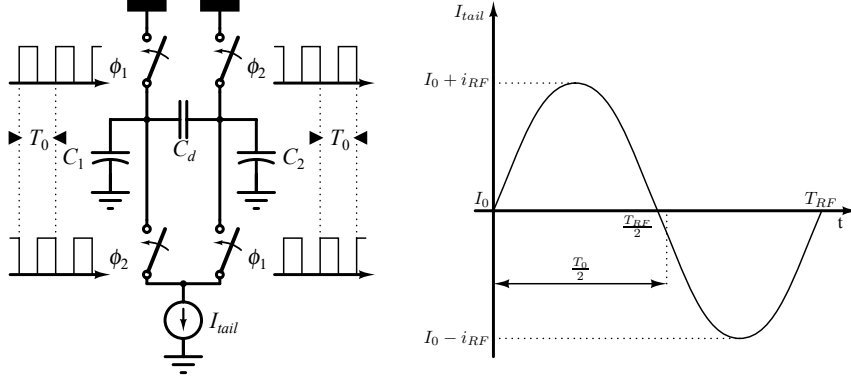


Figure 3.4: SC-theory applied to the LMV cell.

where  $Q$  is the quality factor of inductor  $L_{tank}$ . To complete the analysis, we notice that the capacitance  $C_d$  is in parallel to the effective resistance  $R_{IF}$ , therefore the complete transfer function can be expressed as follows:

$$\frac{v_{IF}}{i_{RF}} \approx \frac{2}{\pi} \frac{R_{IF}}{1 + sC_d R_{IF}}. \quad (3.10)$$

The last equation helps us to determine an upper limit for the GBWP of the stage.

### 3.2 Parasitics-related losses

We want to evaluate the impact of parasitic capacitance  $C_p$ . Since we treat transistors  $M_1 - M_4$  as ideal switches, we can greatly simplify the circuit by applying the theory of switched capacitors (SC). As a further simplification, we consider the impedance of the tank negligible. The simplified structure is depicted in Figure 3.4, where obviously we have  $C_1 = C_2 = C_p$ . In this case we are interested in the RF signal injected by  $I_{tail}$ , therefore the DC component  $I_0$  is disregarded. During a phase (for example  $\phi_1$ ) the

input current injects a certain amount of charge  $Q_{in}$  in the system:

$$Q_{in} = \int_0^{\frac{T_0}{2}} (I_{tail}(t) - I_0) dt \quad (3.11)$$

$$= i_{RF} \int_0^{\frac{T_0}{2}} \sin(\omega_{RF} t) dt = i_{RF} \int_0^{\frac{T_0}{2}} \sin \frac{2\pi t}{T_{RF}} dt \quad (3.12)$$

$$\approx i_{RF} \int_0^{\frac{T_0}{2}} \sin(\omega_0 t) dt = \frac{2i_{RF}}{\omega_0}. \quad (3.13)$$

This charge is going to be shared by  $C_d$  and  $C_2$ . During the (instantaneous) transition  $\phi_1 \rightarrow \phi_2$ , capacitor  $C_2$  is discharged, and the charge  $Q_d$ , already present on  $C_d$ , is redistributed partially on  $C_1$ . At this point we can repeat for phase  $\phi_2$  the same steps (of course  $C_1$  and  $C_2$  have opposite roles): the input RF current has opposite sign now, but it is injected on the opposite side. A detailed sequence is depicted in Figure 3.5. Given the periodic nature of the system, the entire behavioural analysis boils down to a single discrete-time dynamic equation:

$$Q_d(n+1) = \overbrace{(1-\alpha)Q_d(n)}^{\text{redistribution of the charge}} + \overbrace{(1-\alpha)Q_{in}(n)}^{\text{sharing of the input charge}}, \quad (3.14)$$

where  $\alpha \triangleq \frac{C_p}{C_p + C_d}$ . In the  $\mathcal{Z}$ -domain we can rewrite (3.14) as follows:

$$zQ_d(z) = (1-\alpha)[Q_d(z) + Q_{in}(z)], \quad (3.15)$$

$$\mathcal{H}(z) \triangleq \frac{Q_d(z)}{Q_{in}(z)} = \frac{1-\alpha}{z-1+\alpha}. \quad (3.16)$$

We can easily perform a proper mapping from the  $\mathcal{Z}$ -domain to the Laplace-domain; since we are interested in frequencies close to DC, we can approximate the mapping function as follows:

$$z = e^{\frac{sT_0}{2}} \approx 1 + \frac{sT_0}{2} \implies \mathcal{H}(s) = \frac{1-\alpha}{\alpha + \frac{sT_0}{2}}. \quad (3.17)$$

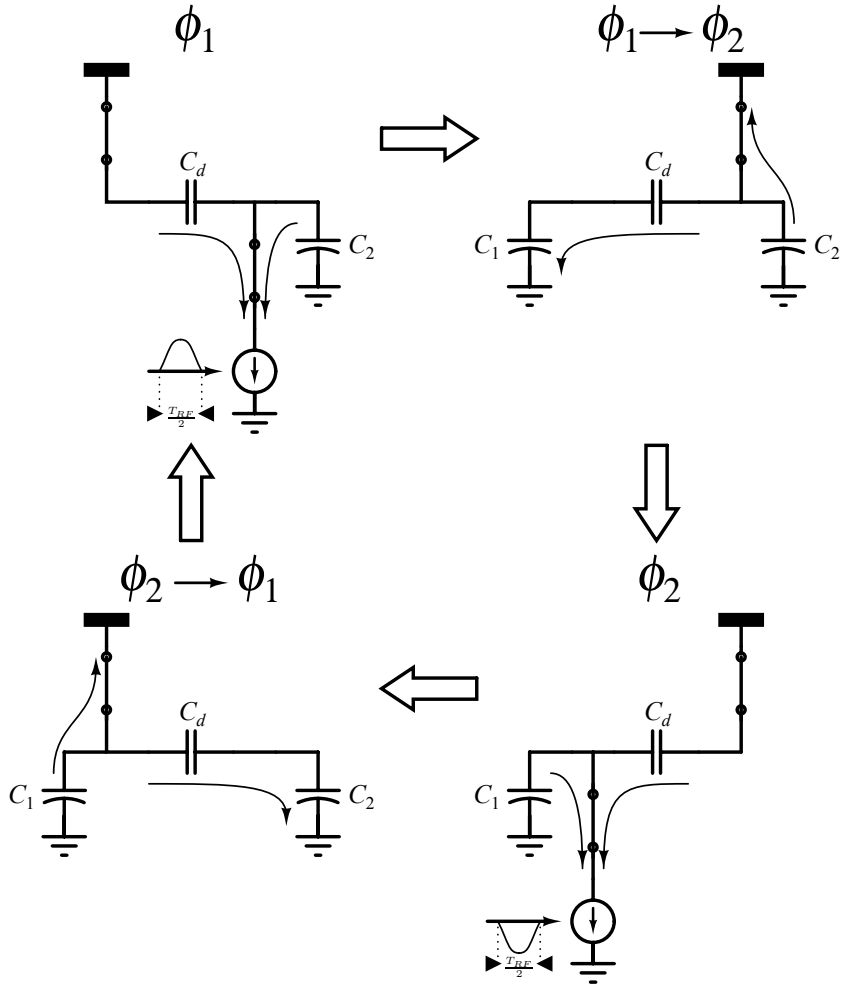


Figure 3.5: Complete cycle  $\phi_1 - \phi_2$ . Different charge-discharge processes are indicated.

From (3.13) and (3.17) we derive the total transfer function:

$$\left. \begin{aligned} Q_{in} &\approx \frac{2i_{RF}}{\omega_0} \\ Q_d &= C_d \cdot v_{IF} \end{aligned} \right\} \frac{v_{IF}}{i_{RF}} \approx \frac{2}{\omega_0 C_d} \cdot \frac{1 - \alpha}{\alpha + \frac{sT_0}{2}} \quad (3.18)$$

$$\approx \frac{2}{\omega_0} \cdot \frac{1 - \alpha}{\alpha C_d} \cdot \frac{1}{1 + \frac{sT_0}{2\alpha}} \quad (3.19)$$

$$\approx \frac{2}{\omega_0 C_p} \cdot \frac{1}{1 + \frac{sT_0}{2\alpha}}. \quad (3.20)$$

We notice that the transfer function in (3.20) has a diverging behaviour for  $C_p \rightarrow 0$ : this stems from the fact that the lossy mechanism described in Section 3.1 is not taken into consideration here.

All in all, equations (3.10) and (3.20) provide reasonable asymptotic bounds for the GBWP of the stage, as it is shown in Section 3.3. In Appendix C we try to provide a unified formulation which embraces the SC-based approach leading to (3.20), and to give a more rigorous explanation for the effective resistance described in Section 3.1.

### 3.3 Numerical results

To prove the validity of limits (3.10) and (3.20) we perform simulations of the LMV structure in semi-ideal conditions:

- MOS transistors are stripped-down of their main capacitive parasitics, in order to resemble ideal switches as much as possible,
- current source  $I_{tail}$  is ideal,
- the LC tank is implemented as an ideal centre-tapped inductor, in which the mutual coupling between the two branches is equal to unity.

We write the transfer function as follows:

$$\frac{v_{IF}}{i_{RF}} = \frac{R_{\text{gain}}}{1 + \frac{s}{BW_{-3\text{dB}}}}. \quad (3.21)$$

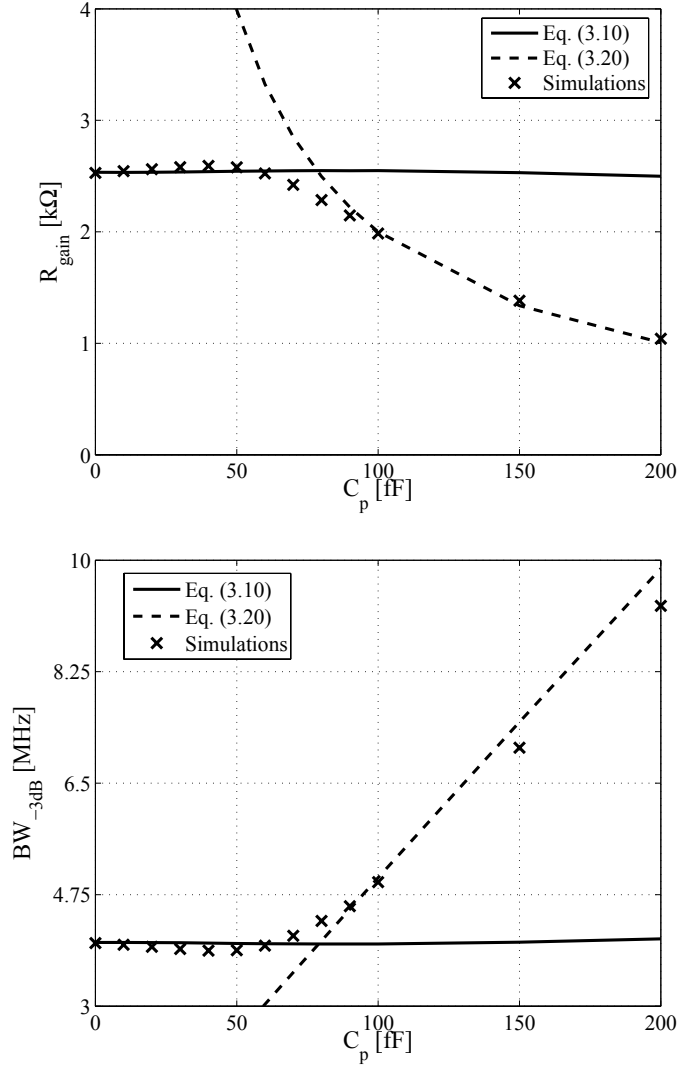


Figure 3.6: Calculation results from (3.10) and (3.20) (continuous and dashed lines respectively) together with simulation results (“x” markers). The low-frequency gain (on top) and the -3dB bandwidth (bottom) are shown.

Table 3.1: Main parameters for results in Figure 3.6.

$f_0$	1.6GHz
$I_0$	1mA
$L_{tank}$	5nH
$Q@f_0$	20
$C_d$	10pF

It is then easy to extract parameters  $R_{\text{gain}}$  and  $BW_{\text{3dB}}$  from simulations using PSS+PAC analyses in Cadence.<sup>®</sup> Results are plotted in Figure 3.6, whereas main parameters are summarized in Table 3.1: we can appreciate that asymptotic curves from (3.10) and (3.20) follow the simulations quite closely in the peripheral regions, and the transition between (3.10)- and (3.20)-regime (which happens for  $C_p \sim 50 \div 100 fF$  in the figure) is very sharp. As predicted by (3.20), the roll-off of  $R_{\text{gain}}$  as a function of  $C_p$  is extremely fast, and this makes this structure rather prone to degradation in performance due to parasitics. To alleviate the problem substantially, a current-mode output is chosen in practical implementations: it can be proven that performance degradation due to parasitic capacitance  $C_p$  is radically reduced [66].

### 3.4 Current-mode output stage

A simple current-mode output stage is depicted in Figure 3.7a; the fully-differential operational amplifier should be able to drive a relatively low resistance, therefore a topology based on a super-cascode stage is preferred (see Figure 3.7b). In order to reduce the required voltage headroom, a self-biased active load is chosen: the final configuration is drawn in Figure 3.7c, where capacitor  $C_{out}$  provides additional low-pass filtering. The fully-differential op-amp schematic is reported in Figure 3.8 (biasing details are simplified). The basic circuit (a) consists of

- a differential pair  $M_7 - M_8$ ,



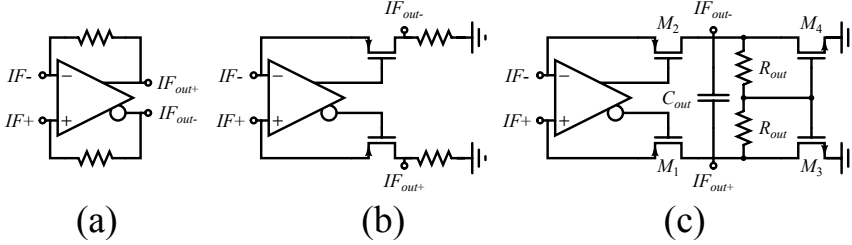


Figure 3.7: A current-mode output stage: simple solution (a), super-cascode with passive load (b) and active load (c).

- an active load  $M_5 - M_6$ ,
- a cascode stage  $M_9 - M_{10}$  followed by
- a self-biased active load  $M_{11} - M_{12} - R_{load}$ .

This folded-cascode topology makes the most out of the reduced supply voltage, but the fully differential circuitry requires a common-mode feedback (CMFB) loop, which is sketched in Figure 3.8b. Very large resistors ( $R_a > 100k\Omega$ ) are used in order to sense the DC voltage at the inputs and feed it into the loop. A basic amplifier *OpAmp2* performs the comparison with the reference voltage  $V_{ref}$  in order to provide the required bias voltage  $V_{bias2}$  to pair  $M_5 - M_6$ . This solution provides reasonable phase margin, even though the gate of  $M_5 - M_6$  is a high-gain node; the filter  $R_b - C_b$  offers one extra degree of freedom to adjust the open-loop frequency-response of the CMFB. Referring again to Figure 3.7c, we notice one additional problem: super-cascode transistors  $M_1 - M_4$  must be biased with a current which is directly *spilled* from the bias current of VCO's core. Therefore, such bias current must be determined accurately, and for this reason reference voltage  $V_{ref}$  must be generated internally. The complete schematic is displayed in Figure 3.8c: devices  $M_{1a} - M_{4a}$  are a replica of the super-cascode stage  $M_1 - M_4$ , they are biased with an adjustable reference current  $I_{bias2}$ , and the source of  $M_{1a} - M_{2a}$  provides the correct  $V_{ref}$ . *OpAmp2* is a simple differential pair with an active load ( $M_{13} - M_{16}$  in the figure). A summary of measured results for the LMV in [1] is presented in Table 3.2, together with simulated parameters for the amplifier in Figure 3.8; the micrograph of the chip is reproduced in Figure 3.9, and some measurement results are reported in Figure 3.10.

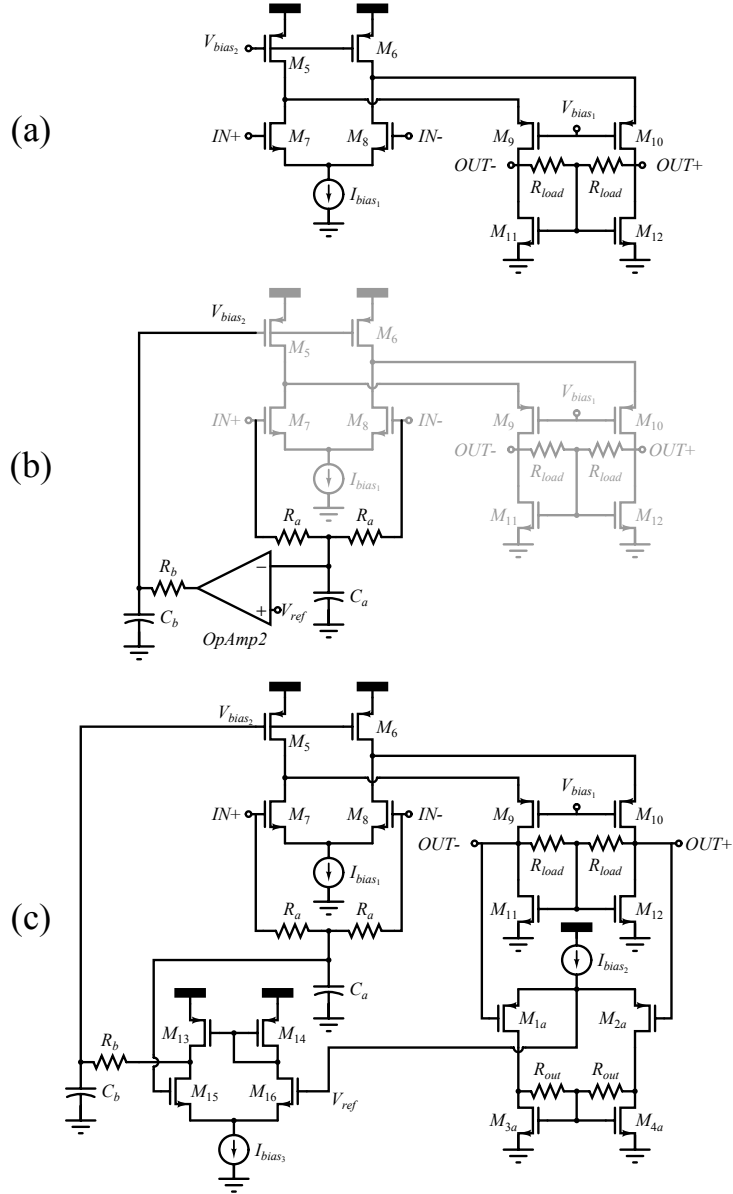


Figure 3.8: Op-Amp schematic: simplified circuit (a), CMFB loop in evidence (b) and complete schematic (c).

Table 3.2: Summary of measured parameters.

LMV cell in [1]	
Gain	36dB
NF (3÷5MHz)	4.8dB
IIP <sub>3</sub>	-19dBm
CP <sub>1dB,out</sub>	-31dBm
PN@1MHz	-104dBc/Hz
I <sub>bias</sub>	4.5mA
V <sub>DD</sub>	1.2V
Amplifier in Figure 3.8	
Gain	35dB
GBWP	135MHz
$\sqrt{\langle i_{n,in}^2 \rangle}$	4.25nA/ $\sqrt{\text{Hz}}$
$\phi_m$ (CMFB loop)	68°

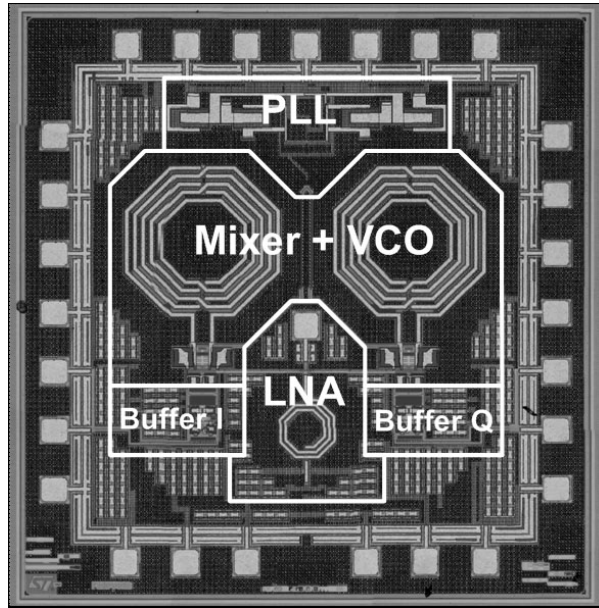


Figure 3.9: Micrograph of the chip presented in [1].

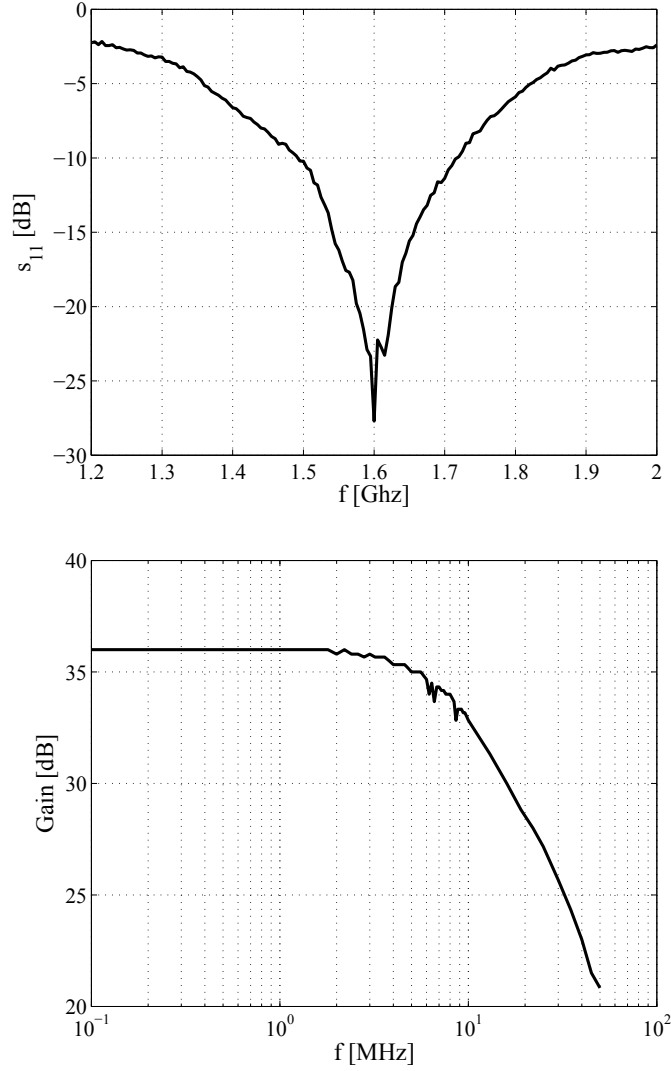


Figure 3.10: Measurement results from [1]:  $s_{11}$  plot (top) and conversion gain (bottom). Input reflection coefficient is lower than -10dB in the range 1.5÷1.7GHz, and  $BW_{-3dB} \approx 10\text{MHz}$ .



## CHAPTER 4

# Toroidal inductors in standard CMOS processes

---

Planar spiral inductors are key passive components in any integrated RF design [16]. In Table 4.1 several implementations from the present *state-of-the-art* are summarized, and we can see that these components are extremely area-hungry; recently it has been proposed to mitigate this issue by integrating active components underneath [83][84], but such coils have anyway the strong tendency to induce RF currents into the substrate. In some applications, magnetic field confinement might be needed, especially when large systems with several different coils are integrated on the same die: mutual interference between coils is likely going to jeopardize overall performances. In this sense, solenoid-based inductors can be a handy choice, and toroidal geometry is definitely preferable because it is very compact and symmetrical: even the internal area can be actively used. Good properties of toroidal inductors have been exploited in advanced micromachining processes [85], but CMOS processes present much different issues. In the following pages a possible approach to toroids' integration is presented: the aim of this implementation is not competing in terms of performances, but rather demonstrating the feasibility of this kind of

Table 4.1: Performance of integrated inductors in CMOS-compatible technologies.

	Area [ $\mu\text{m}^2$ ]	L [nH]	Q@f <sub>peak</sub>	Technology	
[67]	180×180	0.127	48@10GHz	0.25 $\mu\text{m}$	
[68]	240×240	4	22@5GHz	N/A	
[69]	120×120	2	11.2@5GHz	0.25 $\mu\text{m}$	
[70]	N/A	2	8@2GHz	0.25 $\mu\text{m}$	<sup>1</sup>
[71]	300×300	5.6	9@2.4GHz	0.18 $\mu\text{m}$	<sup>2</sup>
[72]	160×200	1.3	15@8GHz	0.35 $\mu\text{m}$	
[73]	21×21	0.42	>15@50GHz	0.13 $\mu\text{m}$ SiGe	
[74]	390×390	2.3	34@7.5GHz	90nm	<sup>1</sup>
[75]	N/A	3	10.8@3.5GHz	0.18 $\mu\text{m}$	
[76]	N/A	3.4	15.7@2.45GHz	0.13 $\mu\text{m}$	<sup>3</sup>
[77]	N/A	0.93	24.9@5GHz	0.13 $\mu\text{m}$	
<i>ib.</i>	N/A	3.5	16@2.4GHz	0.13 $\mu\text{m}$	
[78]	N/A	N/A	16@6GHz	0.35 $\mu\text{m}$	
[79]	380×380	1.8	41@5GHz	90nm	<sup>1</sup>
[80]	825×825	1	51@1GHz	N/A	<sup>4</sup>
[81]	165×165	2	12@10.5GHz	90nm	
[82]	232×232	1.1	>13@20GHz	0.13 $\mu\text{m}$	

<sup>1</sup> The coil is not exactly integrated on the die, therefore area consumption is not an issue, but the WLP technology is nonetheless compatible with CMOS processing.

<sup>2</sup> The dimensions of the coil are estimated by inspecting the die micrograph.

<sup>3</sup> SOI processing is applied.

<sup>4</sup> A CMOS-compatible post-processing is applied.

solution, with respect to obvious technology limitations. The figures summarized in Table 4.1 reveal that planar coils are quite effective in terms of quality factor, which is the ultimate bottle-neck in the vast majority of RF designs. Nevertheless, cross-talking can become a serious issue in the future, since nanometre-scale technologies offer the possibility to integrate larger and larger systems on the same die. Under this perspective, field-confinement properties of toroidal inductors become appealing, also because internal area might be effectively utilized.

## 4.1 Physical implementation

The structure resembles a rectangular-section toroid, and the windings are evenly spaced along the circle. The single winding is built by using the top metal layer running along the radius, a stack of vias going down to the bottom metal level, the bottom metal layer itself running along the radius in the opposite direction, and another stack of vias to get back at top metal level. A graphical representation can be seen in Figure 4.1. Planar inductors can be accurately characterized by means of 2.5D electro-magnetic simulations: the structure is basically extended over 2 dimensions, and this hugely simplifies the analysis. In the case of toroids, pure 3D analysis is necessary, since the structure itself is not planar. Nevertheless the dimensions involved are extreme, since the total area is in the order of fractions of  $mm^2$ , whereas the distance between close windings can be as small as a few  $\mu m$ : simulations might be extremely slow and compromises must be accepted in terms of accuracy. Some qualitative analysis can be performed, though. Figure 4.2 shows a possible setup: the 3D structure is enclosed into a box (resembling the oxide), and the two terminals are driven out for probing on opposite sides of the box, on top and bottom. The negative terminal (together with the bottom plane of the box) is grounded, whereas the positive terminal is driven with a probing signal (basically a constant voltage). The toroid (on the left) is compared with a 2-turn square planar inductor (on the right), which occupies roughly the same area and should provide (according to design kit models) approximately the same inductance. This setup has been simulated with a 3D finite-elements simulator (COMSOL Multiphysics<sup>TM</sup>) in order to provide a qualitative analysis of the structure with respect to the most significant property: field confinement. The normal component of the magnetic field is plotted in magnitude on the silicon plane (in the middle of the picture) and on the cross section



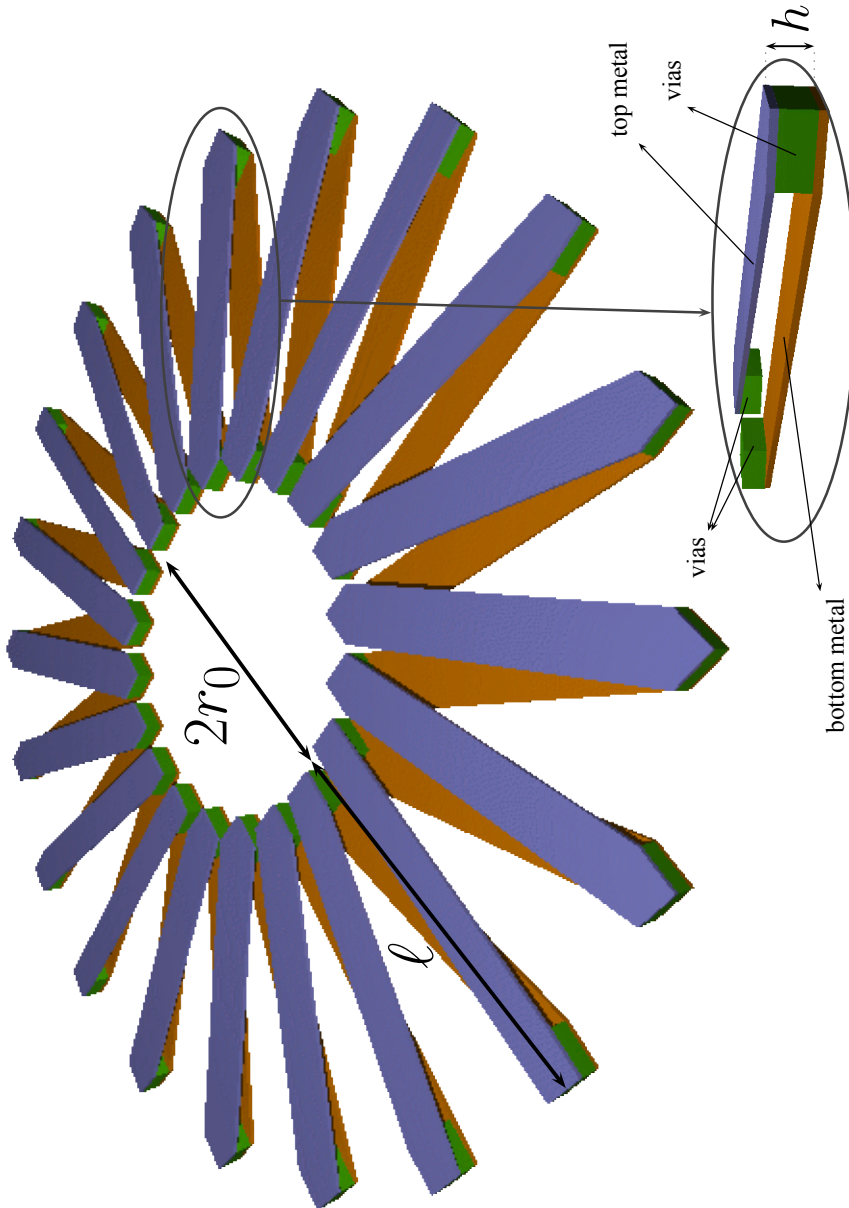


Figure 4.1: 3D representation of the complete structure.

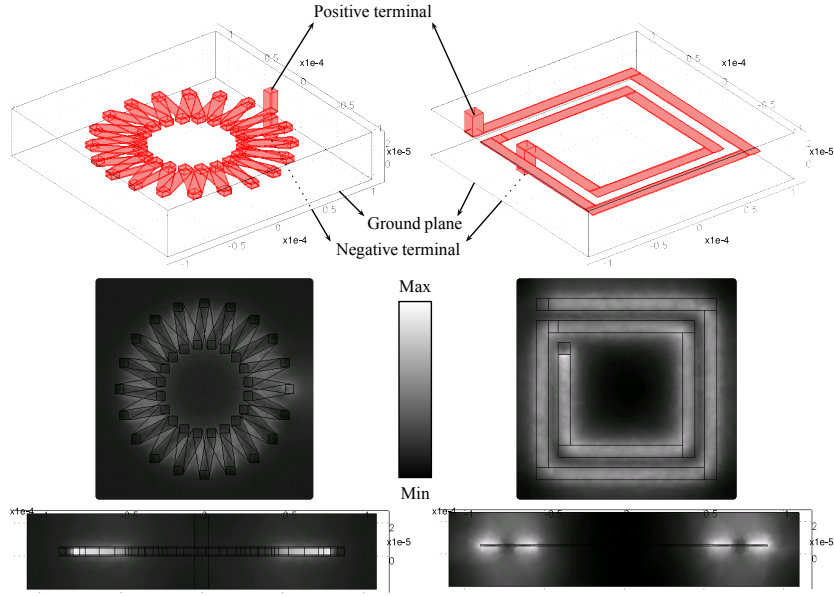


Figure 4.2: 3D representation of a finite-elements simulation setup (on top) together with the results, that show the distribution of the magnetic field magnitude along the silicon plane (middle) and the cross-section (bottom), for the toroidal structure (left) and a reference planar inductor (right).

(at the bottom): the simulation shows that the field is reasonably enclosed in the toroid, especially when compared with the planar spiral inductor. A close-up plot, shown in Figure 4.3, reveals that the field is actually running along the path inside the toroid. In the following, we try to exploit these properties and investigate the behaviour of the component through simple straightforward calculations.

## 4.2 Modelling

Two different approaches are examined in order to analyze the structure and provide reasonable design guidelines. The aim is not providing an accurate model, but rather clear indications about different trade-offs.

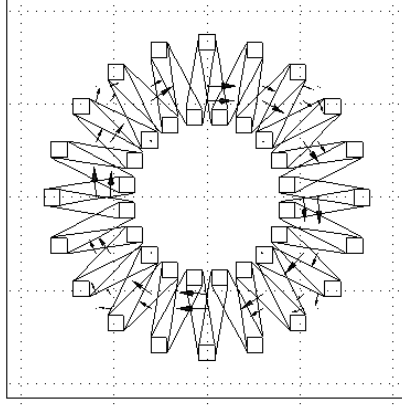


Figure 4.3: Magnetic flux density simulation along the silicon plane for the toroidal inductor.

#### 4.2.1 Classical approach

An air-core rectangular-section toroidal inductor can be easily modelled by means of static Maxwell's equations. A straightforward calculation leads to a well known value for the inductance:

$$L_{coil} = \frac{\mu_0 h}{2\pi} n^2 \log \left( \frac{r_0 + \ell}{r_0} \right), \quad (4.1)$$

where

$\mu_0$  is the magnetic permeability in air (the core is actually built with multilayer oxide, but magnetic properties do not change significantly);

$h$  is the height of the rectangular section of the toroid, as distance between top and bottom metal layers;

$n$  is the number of windings;

$r_0$  is the internal radius of the toroid;

$\ell$  is the difference between external and internal radius.

The calculations are carried on under rather restrictive assumptions:

1. wire dimensions are negligible;
2. flux dispersion outside the toroid is very low;
3. magnetic field is constant along toroid symmetry axis.

None of them is actually verified in this case, but we might get some useful indications anyway. The square dependency shown in (4.1) is very appealing: very high  $Q$  values could be achieved with many windings, since the resistance is growing linearly with  $n$ . However, in practical implementations the physical dimensions must be considered. A major shortcoming for this kind of structure would be the dominant impact of contact resistance associated with vias. In fact, the availability of copper vias is a necessary precondition for the implementation of the coil. In the rest of this section we will consider only the contribution associated with the metal lines, but we will bear in mind that in practice that contribution can be as important as the contact resistance (if not even *less* important). With this simplification we get a total DC resistance

$$R_{\text{DC}} \approx 2\bar{R}_{\square} \frac{\ell}{w} n, \quad (4.2)$$

where  $\bar{R}_{\square}$  is the average metal sheet resistance in  $\Omega/\square$ , and  $w$  is the width of the metal stripe. Furthermore, windings cannot be infinitely close to each other; if  $s$  is the minimum spacing between close lines, we can pack the windings as much as possible, but ultimately we get:

$$2\pi r_0 \approx n(w + s) \Rightarrow n \approx \frac{2\pi r_0}{w + s}. \quad (4.3)$$

Combining equations (4.1), (4.2) and (4.3) and assuming a simple expression for the impedance ( $Z(j\omega) \approx R_{\text{DC}} + j\omega L_{\text{coil}}$ ), we can find a compact and elegant expression for the quality factor normalized with respect to the frequency:

$$\frac{Q}{\omega} \approx \frac{L_{\text{coil}}}{R_{\text{DC}}} \approx \frac{\mu_0 h}{2\bar{R}_{\square}} \cdot \frac{w}{w + s} \cdot \frac{\log\left(1 + \frac{\ell}{r_0}\right)}{\frac{\ell}{r_0}}. \quad (4.4)$$

This final result shows that performances are basically limited by technology, because the upper limit for (4.4) is in any case  $\mu_0 h / 2\bar{R}_{\square}$ . Some marginal optimization can be achieved using wide and short metal stripes. The design parameters in Table 4.2 lead to an inductance value of  $\sim 0.3nH$ .

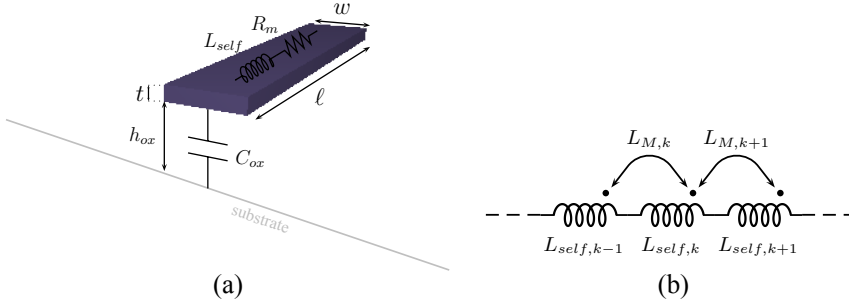


Figure 4.4: A single metal stripe with related parameters (a) and a series of mutually-coupled inductors (b).

#### 4.2.2 Local approach

A self-inductance is associated with the field generated locally by each metal line [86]. This self-inductance can be approximated by means of a widely used expression:

$$L_{\text{self}} = \frac{\mu_0}{2\pi} \ell \left[ \log \left( \frac{2\ell}{w+t} \right) + 0.50049 + \frac{w+t}{3\ell} \right], \quad (4.5)$$

where  $\ell$  is the length of the line,  $w$  is the width and  $t$  is the thickness, as shown in Figure 4.4(a). This approach is extremely versatile, because mutual correlations between neighbours can be calculated as well; the final expression for the total inductance will be in the form:

$$L = \overbrace{\sum_{k=1}^N L_k}^{\text{self}} + \overbrace{\sum_{k \neq j} L_{k,j}}^{\text{mutual}}. \quad (4.6)$$

where  $N$  is the number of metal lines. For example, in Figure 4.4(b) we can see a special case where mutual coupling is considered only between adjacent lines, leading to a total inductance which is still linearly dependent with respect to the number of windings. The expressions in [86] are tailored around a planar structure, nevertheless it might be possible to consider special correction factors in order to accommodate a full 3D structure like the toroid. Such kind of approach has been followed [85] with a good matching between experimental results and numerical model. To get quick

indications, we shall try to focus on fundamental results. The most important fact is that the total inductance is basically linear with respect to the number of metal stripes, and therefore to the number of windings  $n$ . We choose not to consider any kind of mutual effect, as a first-order approximation. Referring to a single metal line as in Figure 4.4(a), we define  $L_{\text{self}}$  as in (4.5), and

$$R_m \approx R_{\square} \frac{\ell}{w}, \quad (4.7)$$

where  $R_{\square}$  has appropriate values for top and bottom metal layers. Based on these assumptions, we find out some indications for the final design: metal lines should be wide and long.

### 4.3 Design

As previously shown, the two modelling approaches provide different indications, but the first one is not applicable in this case, because it's based on assumptions that are not verified; we shall focus on the indications from the second approach. We can simplify the calculations considering a single turn, since no mutual coupling between turns is considered. Resistance from vias stacks should be added to the total resistance, and then some capacitance should be considered in order to estimate self-resonance. Stray capacitance between turns can be easily neglected, as the main contribution comes from bottom metal-to-substrate capacitance. The expression for the single stripe is straightforward:

$$C_{ox} = \epsilon_{ox} \frac{w\ell}{h_{ox}}, \quad (4.8)$$

where  $\epsilon_{ox}$  is the effective dielectric constant of the oxide, and  $h_{ox}$  is the distance between the bottom plate and the substrate. The expression is valid for bottom metal lines, since we consider  $C_{ox} = 0$  for top metal lines. In order to dimension a test-coil, we decide to follow some general guidelines:

- the total inductance should be relatively large ( $L \gtrsim 1nH$ ), otherwise de-embedding the parasitics can produce misleading results,

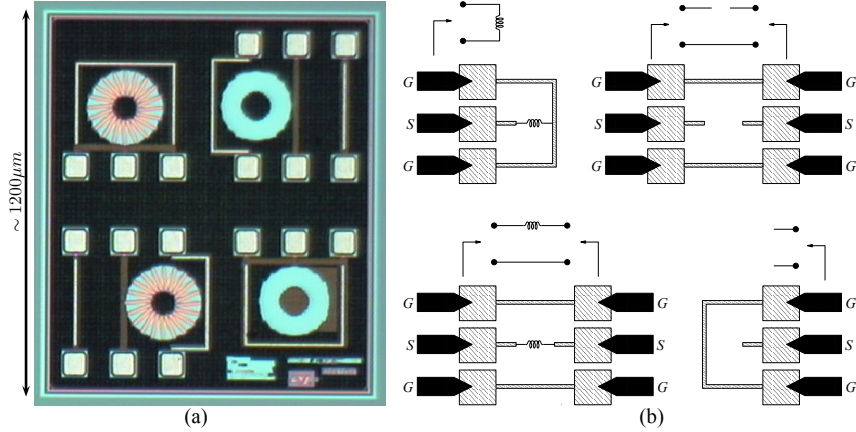


Figure 4.5: Micro photograph of the die (a) and measurement setups (b). From the upper-left quadrant, clockwise: 1-port test setup, 2-port de-embedding setup, 1-port de-embedding setup, 2-port test setup.

- parasitic capacitance should not limit the self-resonance too much (a reasonable target is  $f_{\text{self}} \gtrsim 5GHz$ ),
- DC resistance should of course be minimized.

In addition, regular design rules for CMOS processes must be followed. For example, arbitrarily wide metal lines cannot be fabricated. Design choices and estimated parameters are summarized in Table 4.2. The physical layout of the device is particularly complicated because of the geometry of the toroid itself. It is useful to build a parametric automated procedure to perform all the drawing steps; for the details, see Appendix D. The complete silicon die can be seen in Figure 4.5a. It has been fabricated in a standard CMOS  $0.13\mu m$  process with 6 copper metal lines and copper vias.

## 4.4 Measurement approach and results

The measurements are carried directly on the die by means of standard Ground-Signal-Ground (GSG) microprobes. A 1-port and a 2-port mea-

surement setup is provided on each die (even though only 2-port measurements are used in practice for data analysis, 1-port measurements are useful for quick checks), together with de-embedding counterparts, in order to rule out contributions from pads and parasitics. De-embedding is accomplished by means of an open-circuit structure, as shown in Figure 4.5b. Data analysis is carried on through manipulation of admittance parameters, since the de-embedded values are given by a simple difference:

$$\mathbf{Y}_{\text{dut}}(\omega) = \mathbf{Y}_{\text{dir}}(\omega) - \mathbf{Y}_{\text{de}}(\omega), \quad (4.9)$$

where

$\mathbf{Y}_{\text{dut}}(\omega)$  is the de-embedded result,

$\mathbf{Y}_{\text{dir}}(\omega)$  is the measured admittance matrix of the coil,

$\mathbf{Y}_{\text{de}}(\omega)$  is the measured admittance matrix of the open-circuit de-embedding structure.

This approach provides reasonable results, though some limitations exist:

- short-circuit de-embedding is not performed, and this might have a significant impact especially on  $Q$  factor measurements [87]. The quality factor is going to be underestimated, but previous implementations in older technologies demonstrated that the underestimation is not dramatic;
- the inductor itself can shield the pads [88], but for the sake of simplicity we chose not to perform any calibration aimed to alleviate this issue. Because of this effect, the  $Q$  factor will suffer further underestimation.

To get a closer insight, the idea is to build a very simple  $\Pi$  model like the one showed in Figure 4.6, based on measurement results. Such model is extremely rough, since it does not contain frequency-dependent elements nor mutual couplings, but it is useful in order to make comparisons with hand calculations. More sophisticated approaches can be found in the literature [89].

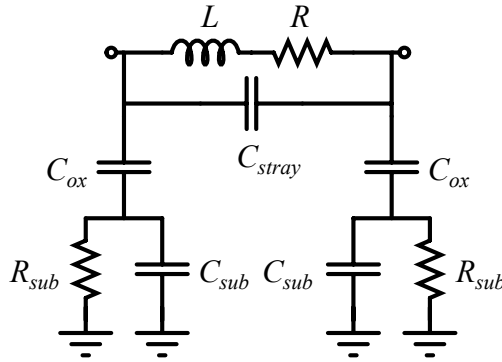


Table 4.2: Design parameters and estimated values.

Param.	Value
$r_0$	$\sim 40\mu m$
$\ell$	$\sim 60\mu m$
$w$	$\sim 12\mu m$
$n$	20
$L$	$\sim 1.4nH$
$R$	$\sim 6.2\Omega$
$C_{ox}$	$\sim 0.45pF$

Table 4.3: Equivalent  $\Pi$  model parameters.

Param.	Value
$L$	$\sim 1.1nH$
$R$	$\sim 6.13\Omega$
$C_{ox}$	$\sim 0.42pF$
$C_{sub}$	$\sim 5fF$
$R_{sub}$	$\sim 115\Omega$
$C_{stray}$	$\sim 2fF$

Figure 4.6: Simple  $\Pi$  model of the inductor.

The procedure is totally empirical: model and measurements data are fed into a simulation tool which applies a straightforward optimization routine to extract the model parameters. The results are summarized in Table 4.3.

It should be easily appreciated the fact that extracted parameters show a good matching with hand calculations already seen in Table 4.2. The inductance itself is easily the most critical parameter, but this is no surprise since we did not account for any mutual correlation between windings. The de-embedded data can be easily manipulated in order to extract relevant performance information. In Figure 4.7 a plot of the  $Q$  factor is shown, together with the effective inductance at different frequencies. We can see a clear trend: the quality factor is increasing as the frequency grows, as

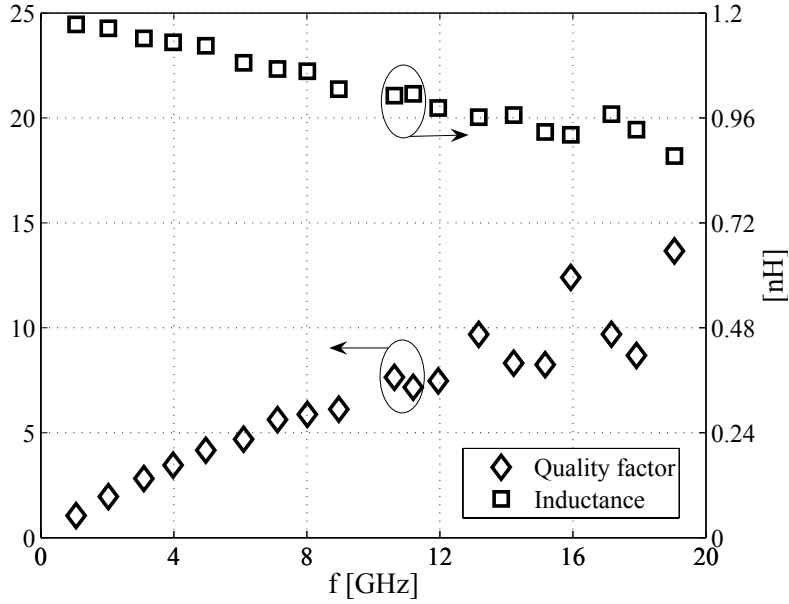


Figure 4.7: Measured  $Q$  factor and inductance of the coil.

anticipated. This means that eddy currents induced in the substrate do not interfere heavily. The inductance value is reasonably constant over the whole range. In Figure 4.8 we can see the real and imaginary part of the impedance, whereas in Figure 4.9 we show the S-parameters on a Smith chart, for 1-port and 2-port measurements. The model is of course not very accurate at high frequencies.

The practical manufacturability of a toroidal inductor with good area-consumption characteristics has been demonstrated. Results show that this implementation cannot challenge a traditional spiral inductors on a performance level, but field confinement properties fulfil the expectations, and high-frequency behaviour suggests that certain applications can greatly benefit from this kind of approach. First-order modelling has been really helpful in the design phase, showing also decent matching with measurements, but nonetheless great improvements can be achieved in this area.

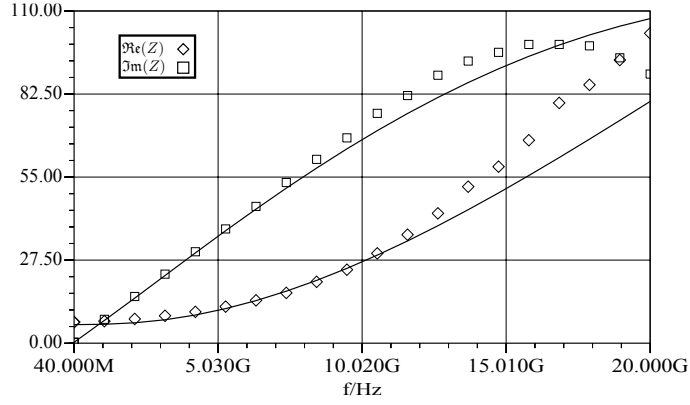


Figure 4.8: One-port measurement of the impedance, shown in terms of real and imaginary part, together with the  $\Pi$ -model approximation (solid lines).

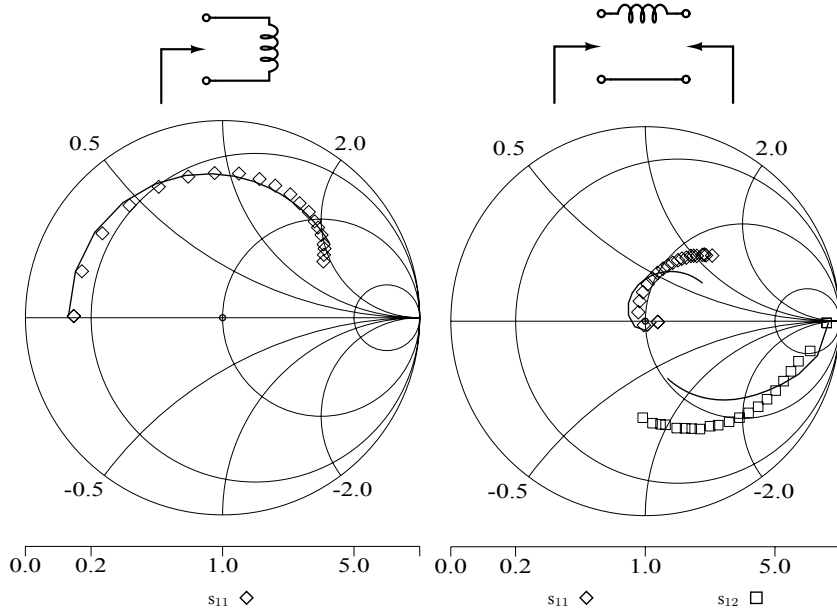


Figure 4.9: S-parameter plots for 1-port and 2-port measurements (on the left and on the right side respectively), together with the  $\Pi$ -model approximation (solid lines).

## Conclusions

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“Σκόπει δὴ, [...] ὦ Κέβης, εἰ ἐκ πάντων τῶν  
εἰρημένων τάδε ἡμῖν συμβαίνει [...];”

“Then reflect, [...] Cebes: is not this the  
conclusion of the whole matter [...];?”

Plato, *Phaedo*

The aim of this work is to exploit the capabilities of CMOS processes for RF applications. The promise of an ever-growing level of integration and interaction with the digital domain is very appealing, and the goal of a full-fledged single-chip radio looks close [90][91]. Portable devices will especially benefit from this (r)evolutionary path: a very compact and low-power structure will embrace several wireless standards at a time, thereby providing multiple functions (e.g. GPS, UMTS, Bluetooth and so on...) with a respectable battery life. In order to offer a wide perspective of the subject, different aspects of RF IC design have been taken into consideration.

The application of negative feedback to the design of RX front-ends has been approached in Chapter 2 on a simulation level. The possibility to embrace a traditional Gilbert-based mixer in the loop without the need for radical circuit modifications has been presented. From this starting point, the concept of dual-loop feedback has been proposed as a viable solution for the very demanding trade-off between input matching, noise and

linearity. A first-order analysis has been performed with the aid of simplified BSIM3 models and detailed calculations: the analysis demonstrates radical linearity improvements, stable performance and reliable noise behaviour. A single-loop narrow-band solution has been introduced as a straight-forward application of the feedback approach: the possibility to improve noise performances (especially for low-performances cheap technologies) has been shown, and a reliable (though very simplified) noise analysis has been sketched and compared with simulations based on the aforementioned models.

Current-reuse techniques can be successfully applied to ultra low-power systems in order to shrink power consumption to the lowest possible limit. A very effective approach has been presented in Chapter 3: the LMV cell efficiently performs the difficult task of integrating an LNA, a mixer and a VCO over the same bias current. A simplified analysis of the structure has been derived, in order to fit the complex trade-offs related to the different blocks sharing the same components. A detailed description of the current-mode output stage has been offered, and measurements results have been summarized, in order to show the remarkable properties of the LMV stage.

In top-performance RF systems the use of integrated inductors is not only a necessity, but an ultimate bottle-neck.<sup>1</sup> As CMOS technology moves on, we can expect improvements in performance and characterization of integrated planar inductors, but the devices remain bulky and difficult to scale, and they present the unpleasant *feature* of inducing strong RF currents in the substrate. An alternative solution has been portrayed in Chapter 4 in the form of a toroidal inductor. The first implementation in CMOS process has been presented, together with a first-order modelling approach and measurements. Overall performances show difficulties in competing with more traditional planar inductors, but the ultimate target of field-enclosure has been achieved without penalties in terms of area consumption.

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<sup>1</sup>“From the point of view of RF circuits, the lack of a good inductor is by far the most conspicuous shortcoming of standard IC processes.” [16]

# Appendices



## APPENDIX A

# Multiplier-based mixers with passive load

---

As we have shown in Chapter 2, node  $v_m$  in Figure 2.1 (the picture is reproduced in Figure A.1 together with the simplified schematic based on the full-switched model) presents an amplified unmodulated replica of the RF

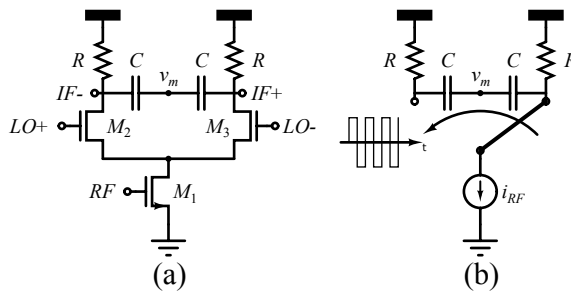


Figure A.1: A down-conversion mixer based on the Gilbert cell: schematic (a) and full-switched model (b).



current signal provided by transconductor  $M_1$ . The fundamental results concerning the down-converted signal and the node  $v_m$  are summarized in equations (2.8)-(2.9), which are reported here for convenience:

$$v_{IF} = -i_{RF} \cdot m_{LO} \cdot \frac{R}{1 + sCR}, \quad (\text{A.1})$$

$$v_m = -i_{RF} \frac{R}{2}. \quad (\text{A.2})$$

The node  $v_m$  is actively used into a feedback topology: if we connect it to another node  $v_b$  in the loop, we must consider the influence of the impedance  $Z_b$  at that node. Referring to Figure A.2, the calculations get a little bit involved, but they can be summarized as follows:

$$Z_h \triangleq \frac{v_h}{i_{in}} = \frac{R \left( \frac{1}{sC} + \frac{Z_b(R + \frac{1}{sC})}{Z_b + R + \frac{1}{sC}} \right)}{R + \frac{1}{sC} + \frac{Z_b(R + \frac{1}{sC})}{Z_b + R + \frac{1}{sC}}}, \quad (\text{A.3})$$

$$Z_t \triangleq \frac{v_t}{i_{in}} = \frac{R \left( \frac{R \cdot Z_b}{Z_b + R + \frac{1}{sC}} \right)}{R + \frac{1}{sC} + \frac{Z_b(R + \frac{1}{sC})}{Z_b + R + \frac{1}{sC}}}, \quad (\text{A.4})$$

$$Z_m \triangleq \frac{v_m}{i_{in}} = \frac{R \frac{Z_b(R + \frac{1}{sC})}{Z_b + R + \frac{1}{sC}}}{R + \frac{1}{sC} + \frac{Z_b(R + \frac{1}{sC})}{Z_b + R + \frac{1}{sC}}}. \quad (\text{A.5})$$

After some manipulation we find out that (A.1) still holds: the output mixing product is unaffected. We can then calculate the voltage at node  $v_m$ :

$$v_m = -i_{RF} \cdot Z_m = -i_{RF} \frac{sCRZ_b}{1 + sC(R + 2Z_b)}. \quad (\text{A.6})$$

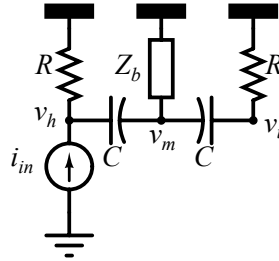


Figure A.2:  $R - C$  low-pass network with buffer input impedance.

Obviously the limit of the previous expression is the same that we found in (A.2):

$$\lim_{Z_b \rightarrow \infty} Z_m = \frac{R}{2}. \quad (\text{A.7})$$

We can evaluate two different situations:

$$Z_b = R_b \Rightarrow Z_m = \frac{sCR R_b}{1 + sC(R + 2R_b)}, \quad (\text{A.8})$$

$$Z_b = \frac{1}{sC_b} \Rightarrow Z_m = \frac{\frac{C}{C_b}}{1 + \frac{2C}{C_b}} \cdot \frac{R}{1 + \frac{sCR}{1 + \frac{2C}{C_b}}}. \quad (\text{A.9})$$

In the first case the transfer function resembles a first-order high-pass filter, whose cut-off frequency is smaller than  $\omega_0 \triangleq \frac{1}{RC}$ . Since  $\omega_0 \ll \omega_{RF}$ ,<sup>1</sup> we can conclude that the transfer at node  $v_m$  is basically flat at the frequencies of interest. This is the most relevant case for the applications presented in Chapter 2. In the second case ( $Z_b = \frac{1}{sC_b}$ ) we have a first-order low-pass filter; the transfer is acceptable as long as the cut-off frequency is reasonably larger than the RF carrier, which means:

$$\omega_1 \triangleq \frac{1 + \frac{2C}{C_b}}{CR} \gg \omega_{RF} \Rightarrow 1 + \frac{2C}{C_b} \gg \omega_{RF} CR. \quad (\text{A.10})$$

Since  $\omega_{RF} CR \gg 1$ , we conclude that  $C_b$  must be extremely small compared to  $C$ .

In practical implementations, the value of resistance  $R$  will be such that the voltage drop across the resistor will be too high. In order to provide a more compact biasing solution, we might think about draining DC current from the tail generator, as in Figure A.3. Solutions (a) and (b) are perfectly equivalent in principle to the original solution shown in Figure A.1a, and therefore all results presented in equations (A.1)-(A.2) hold. There are some differences that can not be seen at a first glance, and solution (b) should perform better in terms of

**switching:** the differential pair must switch a smaller amount of current;

**conversion gain:** the output resistance of the DC current source should be compared with the switching pair input resistance rather than the load resistance  $R$ .

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<sup>1</sup> $\omega_{RF}$  is the RF carrier frequency.

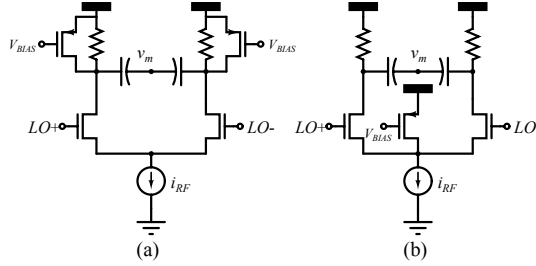


Figure A.3: Ideal mixers with active DC current drain.

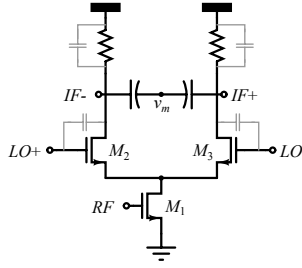


Figure A.4: A resistive-load mixer with parasitic components.

There is another point, that is more subtle. In Figure A.4 we have indicated some critical parasitics that can affect the functionality of the stage. From the point of view of the differential signal  $i_{M_2} - i_{M_3}$  (which is going to be down-converted) parasitic capacitors at nodes  $IF+$  and  $IF-$  provide simply an additional low-pass filtering (at first order); however, the same capacitors attenuate the common-mode signal  $i_{M_2} + i_{M_3}$  and affect the transfer at node  $v_m$  directly. Given a certain capacitance  $C_{par}$  at both nodes, equation (A.2) becomes

$$v_m = -\frac{1}{2} \frac{R}{1 + sRC_{par}}. \quad (\text{A.11})$$

All these considerations lead us to prefer the solution in Figure A.3b, since the influence of parasitics at output nodes should be minimized.

## APPENDIX B

# Nullor-based representation of amplifiers

---

Transmission parameters provide a very convenient way to represent the behaviour of 2-port linear circuits. We can refer to Figure B.1 to define the relationships between relevant signals as follows:

$$\begin{pmatrix} v_{in} \\ i_{in} \end{pmatrix} = \underbrace{\begin{pmatrix} A & B \\ C & D \end{pmatrix}}_{\text{chain matrix}} \cdot \begin{pmatrix} v_{out} \\ i_{out} \end{pmatrix}. \quad (\text{B.1})$$

Transmission parameters  $A$ ,  $B$ ,  $C$  and  $D$  can be reciprocated to obtain *transfer* parameters, somewhat more familiar in electronic design:

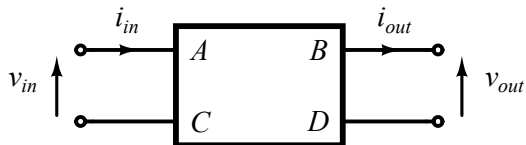


Figure B.1: A 2-port circuit represented by its transmission parameters.

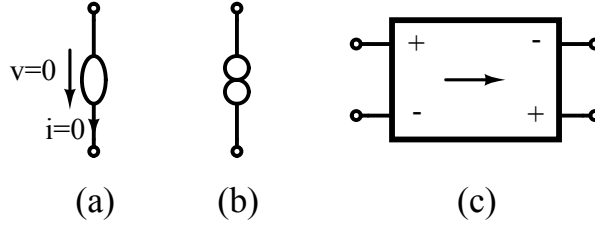


Figure B.2: Symbols of a nullator (a), a norator (b) and a nullor (c).

$$\mu \triangleq \frac{1}{A} = \left. \frac{v_{out}}{v_{in}} \right|_{i_{out}=0} : \text{ voltage gain,}$$

$$\gamma \triangleq \frac{1}{B} = \left. \frac{i_{out}}{v_{in}} \right|_{v_{out}=0} : \text{ transadmittance,}$$

$$\zeta \triangleq \frac{1}{C} = \left. \frac{v_{out}}{i_{in}} \right|_{i_{out}=0} : \text{ transimpedance,}$$

$$\alpha \triangleq \frac{1}{D} = \left. \frac{i_{out}}{i_{in}} \right|_{v_{out}=0} : \text{ current gain.}$$

An ideal amplifier can be represented by means of two components, a *nullator* and a *norator* [92]:

**a nullator** (see Figure B.2a) is an ideal 2-terminal element which enforces both a zero-voltage and a zero-current between its terminals,

**a norator** (see Figure B.2b) is an ideal 2-terminal element which imposes no constraints on its branch current and voltage.

The *nullor* is a combination of a nullator and a norator. Such element is associated with an all-zeros chain matrix:

$$\begin{pmatrix} v_{in} \\ i_{in} \end{pmatrix} = \begin{pmatrix} 0 & 0 \\ 0 & 0 \end{pmatrix} \cdot \begin{pmatrix} v_{out} \\ i_{out} \end{pmatrix}. \quad (\text{B.2})$$

In Figure B.2c the common symbol for the nullor is given. An example of a single-amplifier topology represented with the use of a nullor is given in Figure B.3 [93]. The nullator imposes the same voltage  $v_{in}$  at both its terminals, but no current flows into them. Therefore the current flowing into  $R_1$  is determined entirely by  $v_{in}$ , and the norator determines the

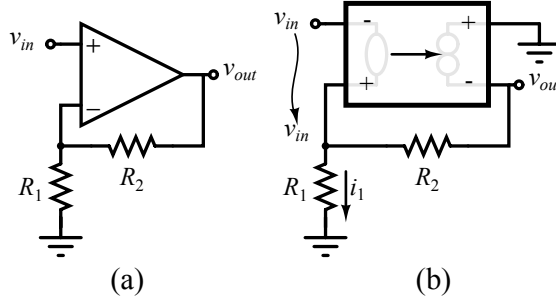


Figure B.3: A conventional operational amplifier used in a non-inverting feedback topology (a) and its representation based on the nullor (b).

output voltage accordingly. The following equations describe the behaviour of the circuit and determines familiar relationships:

$$i_1 = \frac{v_{in}}{R_1},$$

$$v_{out} = v_{in} + i_1 \cdot R_2 = v_{in} \left( 1 + \frac{R_2}{R_1} \right).$$



## APPENDIX C

# A unified approach to the analysis of the LMV cell

---

In Chapter 3 we have performed a simplified analysis of the LMV cell based on two approaches, leading to equations (3.10) and (3.20); such equations describe the behaviour of the stage by means of two different asymptotic scenarios. In the following, we will try to provide a *single* model that accounts for both aspects of the problem. We will modify the approach followed in Section 3.2 in order to accommodate additional lossy mechanisms that limit the GBWP of the stage for low values of parasitic capacitance. The starting point is again Figure 3.4 and Figure 3.5. First of all, we have to examine carefully what happens during transition  $\phi_1 \rightarrow \phi_2$  (and similarly  $\phi_2 \rightarrow \phi_1$ ). Referring to Figure C.1, we consider only the core of the oscillator and we apply a test current  $i_{probe}$ . During the transition, transistors  $M_3 - M_4$  work as current generators, and we can



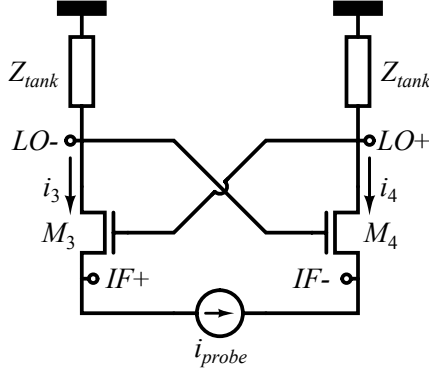


Figure C.1: Evaluation of resistance at the sources of  $M_3$  and  $M_4$ .

sum up all relevant equations as follows:

$$i_3 = g_{m_3}(v_{LO+} - v_{IF+}) \quad (C.1)$$

$$= g_{m_3}(-Z_{tank} \cdot i_4 - v_{IF+}) \quad (C.2)$$

$$= g_{m_3}(Z_{tank} \cdot i_{probe} - v_{IF+}), \quad (C.3)$$

$$i_4 = g_{m_4}(v_{LO-} - v_{IF-}) \quad (C.4)$$

$$= g_{m_4}(-Z_{tank} \cdot i_3 - v_{IF-}) \quad (C.5)$$

$$= g_{m_4}(-Z_{tank} \cdot i_{probe} - v_{IF-}), \quad (C.6)$$

$$G_d \triangleq \frac{i_{probe}}{v_{IF-} - v_{IF+}} = \frac{g_{m_3}g_{m_4}}{g_{m_3} + g_{m_4} - 2g_{m_3}g_{m_4}Z_{tank}}. \quad (C.7)$$

Capacitor  $C_d$  is discharged almost instantaneously, therefore we can approximate (C.7) as follows:

$$G_d \approx \frac{g_{m_3}g_{m_4}}{g_{m_3} + g_{m_4}}. \quad (C.8)$$

Assuming that the discharge is taking place in a very short time interval  $[-\Delta t, \Delta t]$  around the transition instant, the charge loss can be easily

determined:

$$-C_d \frac{dv_{IF}}{dt} = G_d v_{IF} \quad (C.9)$$

$\Downarrow$

$$v_{IF}(\Delta t) = v_{IF}(-\Delta t) e^{-\frac{1}{C_d} \int_{-\Delta t}^{\Delta t} G_d(t) dt}; \quad (C.10)$$

$$\Delta Q_d = C_d v_{IF}(-\Delta t) e^{-\frac{1}{C_d} \int_{-\Delta t}^{\Delta t} G_d(t) dt} - C_d v_{IF}(-\Delta t) \quad (C.11)$$

$$\approx -\frac{Q_d(-\Delta t)}{C_d} \int_{-\Delta t}^{\Delta t} G_d(t) dt, \quad (C.12)$$

We can calculate  $G_d$  explicitly by means of equations (53)-(54) in [94]: they have been derived for a common-source switching pair, but they can fit this analysis at first order.

$$g_{m_3} = k_0 V_0 \left( -\sin \varphi + \sqrt{2 \sin^2 \Phi - \sin^2 \varphi} \right); \quad (C.13)$$

$$g_{m_4} = k_0 V_0 \left( \sin \varphi + \sqrt{2 \sin^2 \Phi - \sin^2 \varphi} \right); \quad (C.14)$$

$$k_0 \triangleq \frac{1}{2} \mu_{n0} C'_{ox} \frac{W}{L}; \quad (C.15)$$

$$\Phi \triangleq \arcsin \sqrt{\frac{I_0}{2k_0 V_0^2}}. \quad (C.16)$$

where  $\varphi \triangleq \omega_0 t$ ,  $\Phi = \omega_0 \Delta t$  is the angle corresponding to time interval  $\Delta t$ , and  $V_0, I_0$  are defined as in Section 3.1. By further processing we find:

$$G_d(\varphi) = k_0 V_0 \frac{\sin^2 \Phi - \sin^2 \varphi}{\sqrt{2 \sin^2 \Phi - \sin^2 \varphi}}, \quad (C.17)$$

$$\begin{aligned} \int_{-\Delta t}^{\Delta t} G_d(t) dt &= \frac{1}{\omega_0} \int_{-\Phi}^{\Phi} G_d(\varphi) d\varphi \\ &\approx k_0 V_0 \frac{\Phi^2}{\omega_0} \\ &\approx \frac{I_0}{2\omega_0 V_0}, \end{aligned} \quad (C.18)$$

$$\Delta Q_d \approx -\frac{Q_d(-\Delta t)}{C_d} \frac{I_0}{2\omega_0 V_0}, \quad (C.19)$$

$$\beta \triangleq \frac{I_0}{2C_d \omega_0 V_0} \implies \Delta Q_d \approx -\beta \cdot Q_d(-\Delta t). \quad (C.20)$$

Since we have determined the charge losses during the transition, we can rewrite (3.14) as follows:

$$Q_d(n+1) = \overbrace{(1-\alpha)(1-\beta)Q_d(n)}^{\substack{\text{redistribution} \\ \text{of the charge} \\ \text{and losses during} \\ \text{the transition}}} + \overbrace{(1-\alpha)Q_{in}(n)}^{\substack{\text{sharing of the} \\ \text{input charge}}}, \quad (\text{C.21})$$

and proceed to determine the total transfer function using the same approximations as above.

$$\mathcal{H}(z) \triangleq \frac{Q_d(z)}{Q_{in}(z)} = \frac{1-\alpha}{z - (1-\alpha)(1-\beta)}, \quad (\text{C.22})$$

$$\mathcal{H}(s) \approx \frac{1-\alpha}{1 + \frac{sT_0}{2} - (1-\alpha)(1-\beta)}, \quad (\text{C.23})$$

$$\frac{v_{IF}}{i_{RF}} = \frac{2}{\omega_0 C_d} \mathcal{H}(s) \approx \frac{2}{\omega_0 C_d} \cdot \frac{1-\alpha}{\alpha + \beta - \alpha\beta} \cdot \frac{1}{1 + \frac{sT_0}{2(\alpha + \beta - \alpha\beta)}}. \quad (\text{C.24})$$

We can easily verify that the following limits hold:

$$\begin{aligned} \beta \gg \alpha &\implies \text{losses due to } C_p \text{ are negligible} \\ &\implies \frac{v_{IF}}{i_{RF}} \approx \frac{2}{\pi} \frac{R_{IF}}{1 + sC_d R_{IF}} \text{ as in (3.10),} \\ \alpha \gg \beta &\implies \text{losses due to } C_p \text{ dominate} \\ &\implies \frac{v_{IF}}{i_{RF}} \approx \frac{2}{\omega_0 C_p} \cdot \frac{1}{1 + \frac{sT_0}{2\alpha}} \text{ as in (3.20).} \end{aligned}$$

In Figure C.2, numerical results from (C.24) are shown together with simulation results (simulation parameters are the same as in Table 3.1, and reproduced in Table C.1 for convenience). It is possible to refine the figures given by (C.24) by means of numerical analysis: referring to Figure C.3, we consider  $Z_{tank} = 0$ , and we write the differential equations at nodes  $IF+$  and  $IF-$ .

$$(C_p + C_d) \frac{dv_{IF-}}{dt} - C_d \frac{dv_{IF+}}{dt} + g_{m4} v_{IF-} = 0; \quad (\text{C.25})$$

$$(C_p + C_d) \frac{dv_{IF+}}{dt} - C_d \frac{dv_{IF-}}{dt} + g_{m3} v_{IF+} = 0. \quad (\text{C.26})$$

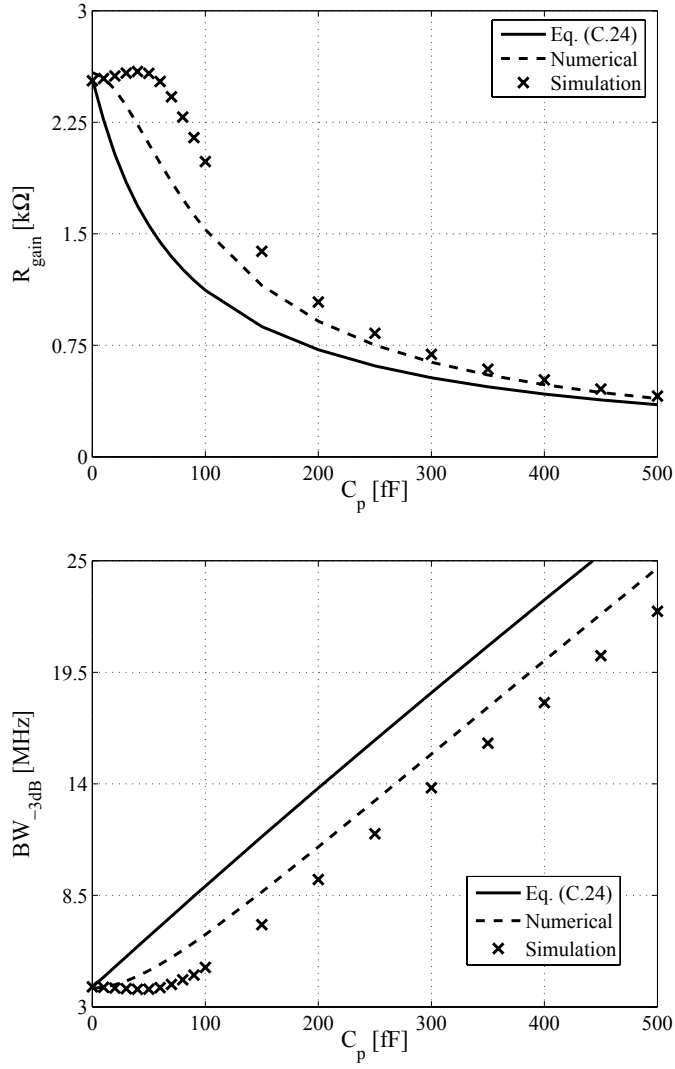


Figure C.2: Calculation results from (C.24) without and with numerical correction (continuous and dashed lines respectively) together with simulation results (“x” markers). The low-frequency gain (on top) and the -3dB bandwidth (bottom) are shown.



## APPENDIX D

# Layout automation based on SKILL scripting language

---

The layout of integrated inductors is a tedious procedure that can be greatly sped up using automated tools. Cadence<sup>®</sup> design environment offers a very advanced scripting language named *SKILL*. A *parametric cell* can be created using this language: once the cell has been added to the design library, the layout tool will prompt the user a single mask containing all customizable parameters, and then it will design the cell according to the input.

In the case of the toroidal inductor described in Chapter 4, we refer to Figure D.1a to determine the sequence of drawing steps. Given a certain number of turns  $n$ , internal radius  $r_0$ , minimum width  $w_s$  and cross-section  $\ell$ , before drawing the pattern for the vias we must check that all metal lines respect the minimum clearance, otherwise the parameter  $r_0$  must be adjusted. Once the pattern is drawn, we can complete the structure with metal lines, as shown in Figure D.1b. In the following pages the *SKILL* code for all the necessary steps is presented. It's preferable to separate the definition of user parameters and the actual design procedure (which in turn can make use of several other procedures).

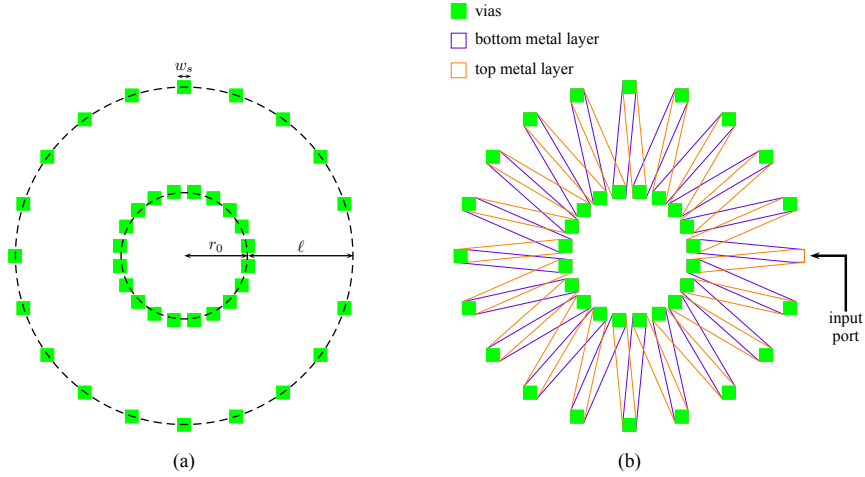


Figure D.1: Top view of the toroid: the pattern for the placement of the vias (a) and the complete structure (b).

### Constants

```
Pi=3.141596
sq2=1.414213562
minGrid=0.005 ; in micrometers
```

This procedure fixes points on the grid

```
procedure(grid(x step)
  step=max( minGrid fix(round(step/minGrid))*minGrid )
  fix(round(x/step))*step
) ;grid
```

A procedure to build multilayer metal connections

```
procedure( rectS( cv w l step x0 y0 layerlist vialist)
  let( ( minw, ; minimum dimensions
    layer, ; index
    nx1, ny1, nx2, ny2, ; number of contacts for each axis
    wvial, dist1, ; VIAs' geometry parameters
```

---

```

wvia2, dist2;; VIAs' geometry parameters
border1, border2;; VIAs' geometry parameters
P0enc ; PADOPEN geometry parameters
)

wvia1 = 0.19
dist1 = 0.29
wvia2 = 0.36
dist2 = 0.54
border1= 0.05
border2= 0.09

P0enc = 0.7

minw = 0

w = max( minw grid( w step ) )
l = max( minw grid( l step ) )

x0 = grid( x0 step )
y0 = grid( y0 step )

foreach( layer layerlist
  if( layer=="alucap"
    then
      dbCreatePolygon( cv list("alucap" "induct")
        list(x0:y0 x0:(y0+w) (x0+l):(y0+w) (x0+l):y0))
    else
      dbCreatePolygon( cv layer
        list(x0:y0 x0:(y0+w) (x0+l):(y0+w) (x0+l):y0))
      ) ; if( layer=="alucap" )
) ; foreach( layer layerlist )

nx1 = fix( (l-2*border1+dist1)/(wvia1+dist1) )
ny1 = fix( (w-2*border1+dist1)/(wvia1+dist1) )
nx2 = fix( (l-2*border2+dist2)/(wvia2+dist2) )
ny2 = fix( (w-2*border2+dist2)/(wvia2+dist2) )

foreach( layer vialist
  if( layer=="M6_M5"
    then
      leCreateContact( cv layer (x0+grid((0.5*l) step)):(y0+grid((0.5*w)
        step)) "R0" wvia2 wvia2 ny2 nx2 (wvia2+dist2) (wvia2+dist2)
"center" "center" )
    else if( layer=="padopen"
      then
        dbCreatePolygon( cv list("padopen" "induct")
          list((x0+P0enc):(y0+P0enc) (x0+P0enc):(y0+w-P0enc)
            (x0+l-P0enc):(y0+w-P0enc) (x0+l-P0enc):(y0+P0enc)))
        else
          leCreateContact( cv layer

```



```

        (x0+grid((0.5*l) step)):(y0+grid((0.5*w) step))
        "R0" wvia1 wvia1 ny1 nx1 (wvia1+dist1) (wvia1+dist1)
        "center" "center" ))
    ) ; multiple if
  ) ; foreach( layer vialist )

  ) ; let

) ; procedure( rectS )

; User interface

pcDefinePCell(
list( ddGetObj( "LV_PCells" ) "rectStack" "layout" )

( (Width float 11.99)
  (Length float 30.0)
  (Grid float 0.005)
  (X0 float 0.0)
  (Y0 float 0.0)
  (metal1 boolean "TRUE")
  (metal2 boolean "TRUE")
  (metal3 boolean "FALSE")
  (metal4 boolean "FALSE")
  (metal5 boolean "FALSE")
  (metal6 boolean "FALSE")
  (alucap boolean "FALSE")
)

cv=pcCellView
layerlist = list( )
vialist = list( )
minlayer = 8
maxlayer = 0

when( metal1 == t
  minlayer = 1
  maxlayer = 1)
when( metal2 == t
  minlayer = min( minlayer 2 )
  maxlayer = max( maxlayer 2 ))
when( metal3 == t
  minlayer = min( minlayer 3 )
  maxlayer = max( maxlayer 3 ))
when( metal4 == t
  minlayer = min( minlayer 4 )
  maxlayer = max( maxlayer 4 ))
when( metal5 == t
  minlayer = min( minlayer 5 )
  maxlayer = max( maxlayer 5 ))
when( metal6 == t

```

---

```

    minlayer = min( minlayer 6 )
    maxlayer = max( maxlayer 6 ))
when( alucap == t
    minlayer = min( minlayer 7 )
    maxlayer = max( maxlayer 7 ))

if( minlayer==1
then
    layerlist = cons( "metal1" layerlist)
) ; if( minlayer==1 )
if( minlayer==2
then
    layerlist = cons( "metal2" layerlist)
) ; if( minlayer==2 )
if( minlayer==3
then
    layerlist = cons( "metal3" layerlist)
) ; if( minlayer==3 )
if( minlayer==4
then
    layerlist = cons( "metal4" layerlist)
) ; if( minlayer==4 )
if( minlayer==5
then
    layerlist = cons( "metal5" layerlist)
) ; if( minlayer==5 )
if( minlayer==6
then
    layerlist = cons( "metal6" layerlist)
) ; if( minlayer==6 )
if( minlayer==7
then
    layerlist = cons( "alucap" layerlist)
) ; if( minlayer==7 )

for( i (minlayer+1) maxlayer
    if( i==2
    then
        layerlist = cons( "metal2" layerlist)
        vialist = cons( "M2_M1" vialist)
    ) ; if( i==2 )
    if( i==3
    then
        layerlist = cons( "metal3" layerlist)
        vialist = cons( "M3_M2" vialist)
    ) ; if( i==3 )
    if( i==4
    then
        layerlist = cons( "metal4" layerlist)
        vialist = cons( "M4_M3" vialist)
    ) ; if( i==4 )

```

```

if( i==5
then
    layerlist = cons( "metal5" layerlist)
    vialist   = cons( "M5_M4" vialist)
) ; if( i==5 )
if( i==6
then
    layerlist = cons( "metal6" layerlist)
    vialist   = cons( "M6_M5" vialist)
) ; if( i==6 )
if( i==7
then
    layerlist = cons( "alucap" layerlist)
    vialist   = cons( "padopen" vialist)
) ; if( i==7 )
) ; for( i (minlayer+1) maxlayer )

layerlist = reverse(layerlist)
vialist = reverse(vialist)

rectS( cv Width Length Grid X0 Y0 layerlist vialist)

) ; pcDefinePCell

```

### A procedure to build multilayer metal connections with 45° rotation

```

procedure( rectS45( cv w l step x0 y0 layerlist vialist)
let( ( minw, ; minimum dimensions
    weff, leff ; effective dimensions
    layer, ; index
    na1, nb1, na2, nb2,; number of contacts for each axis
    wvia1, dist1,; VIAs' geometry parameters
    wvia2, dist2,; VIAs' geometry parameters
    border1, border2 ; VIAs' geometry parameters
    P0enc ; PADOPEN geometry parameters
)

wvia1 = 0.19
dist1 = 0.29
wvia2 = 0.36
dist2 = 0.54
border1= 0.05
border2= 0.09
P0enc = 0.7
P0enc = grid( P0enc*sq2 step )
minw = 4.4
w = max( minw w )

```

---

```

l = max( w l )
x0 = grid( x0 step )
y0 = grid( y0 step )
weff = max( grid( w/sq2 step ) grid( minw/sq2 step ) )
leff = max( grid( l/sq2 step ) grid( minw/sq2 step ) )

foreach( layer layerlist
  if( layer=="alucap"
    then
      dbCreatePolygon( cv list("alucap" "induct") list(x0:y0 (x0-weff):
        (y0+weff) (x0+leff-weff):(y0+leff+weff) (x0+leff):(y0+leff)))
    else
      dbCreatePolygon( cv layer list(x0:y0 (x0-weff):(y0+weff)
        (x0+leff-weff):(y0+leff+weff) (x0+leff):(y0+leff)))
    ) ; if( layer=="alucap" )
  ) ; foreach( layer layerlist )

na1 = fix( (weff-0.5*wvia1+0.5*dist1-2*border1)/(wvia1
  +dist1) )
na2 = fix( (weff-0.5*wvia2+0.5*dist2-2*border2)/(wvia2
  +dist2) )
nb1 = fix( (leff-weff)/(wvia1+dist1) )
nb2 = fix( (leff-weff)/(wvia2+dist2) )

foreach( layer vialist
  if( layer=="M6_M5"
    then
      for( i 1 na2
        leCreateContact( cv layer (x0+leff-weff):(y0+leff+weff-wvia2
          -2*border2-(wvia2+dist2)*(i-1)) "R0" wvia2 wvia2 1 (2*i-1)
          (wvia2+dist2) (wvia2+dist2) "center" "center" )
        leCreateContact( cv layer x0:(y0+wvia2+2*border2+(wvia2
          +dist2)*(i-1)) "R0" wvia2 wvia2 1 (2*i-1) (wvia2+dist2)
          (wvia2+dist2) "center" "center" )
      ) ; for( i 1 na2 )
      for( i 1 nb2
        leCreateContact( cv layer (x0+leff-weff-(i-1)*(wvia2+dist2):(y0
          +leff-dist2+2*border2-0.5*wvia2-(i-1)*(wvia2+dist2)) "R0" wvia2
          wvia2 1 2*na2-1) (wvia2+dist2) (wvia2+dist2) "center" "center" )
      ) ; for( i 1 nb2 )
    else if( layer=="padopen"
      then
        dbCreatePolygon( cv list("padopen" "induct") list(x0:(y0+POenc)
          (x0-weff+POenc):(y0+weff) (x0+leff-weff):(y0+leff+weff-POenc)
          (x0+leff-POenc):(y0+leff)))
        else
          for( i 1 na1
            leCreateContact( cv layer (x0+leff-weff):(y0+leff+weff-wvia1
              -2*border1-(wvia1+dist1)*(i-1)) "R0" wvia1 wvia1 1 (2*i-1)
              (wvia1+dist1) (wvia1+dist1) "center" "center" )
            leCreateContact( cv layer x0:(y0+wvia1+2*border1+(wvia1

```

```

        +dist1)*(i-1)) "R0" wvia1 wvia1 1 (2*i-1) (wvia1+dist1)
        (wvia1+dist1) "center" "center" )
    ) ; for( i 1 na1 )
    for( i 1 nb1
        leCreateContact( cv layer (x0+leff-weff-(i-1)*(wvia1+dist1)):(y0
            +leff-dist1+2*border1-0.5*wvia1-(i-1)*(wvia1+dist1)) "R0" wvia1
            wvia1 1 (2*na1-1) (wvia1+dist1) (wvia1+dist1) "center" "center" )
        ) ; for( i 1 nb1 )
    )
    ) ; multiple if
) ; foreach( layer vialist )

) ; let

) ; procedure( rectS45 )

; User interface

pcDefinePCell(
list( ddGetObj( "LV_PCells" ) "rectStack45" "layout" )

( (Width float 11.99)
  (Length float 30.0)
  (Grid float 0.005)
  (X0 float 0.0)
  (Y0 float 0.0)
  (metal1 boolean "TRUE")
  (metal2 boolean "TRUE")
  (metal3 boolean "FALSE")
  (metal4 boolean "FALSE")
  (metal5 boolean "FALSE")
  (metal6 boolean "FALSE")
  (alucap boolean "FALSE")
)

cv=pcCellView
layerlist = list( )
vialist = list( )
minlayer = 8
maxlayer = 0

when( metal1 == t
    minlayer = 1
    maxlayer = 1)
when( metal2 == t
    minlayer = min( minlayer 2 )
    maxlayer = max( maxlayer 2 ))
when( metal3 == t
    minlayer = min( minlayer 3 )
    maxlayer = max( maxlayer 3 ))
when( metal4 == t

```

---

```

    minlayer = min( minlayer 4 )
    maxlayer = max( maxlayer 4 ))
when( metal5 == t
    minlayer = min( minlayer 5 )
    maxlayer = max( maxlayer 5 ))
when( metal6 == t
    minlayer = min( minlayer 6 )
    maxlayer = max( maxlayer 6 ))
when( alucap == t
    minlayer = min( minlayer 7 )
    maxlayer = max( maxlayer 7 ))

if( minlayer==1
then
    layerlist = cons( "metal1" layerlist)
) ; if( minlayer==1 )
if( minlayer==2
then
    layerlist = cons( "metal2" layerlist)
) ; if( minlayer==2 )
if( minlayer==3
then
    layerlist = cons( "metal3" layerlist)
) ; if( minlayer==3 )
if( minlayer==4
then
    layerlist = cons( "metal4" layerlist)
) ; if( minlayer==4 )
if( minlayer==5
then
    layerlist = cons( "metal5" layerlist)
) ; if( minlayer==5 )
if( minlayer==6
then
    layerlist = cons( "metal6" layerlist)
) ; if( minlayer==6 )
if( minlayer==7
then
    layerlist = cons( "alucap" layerlist)
) ; if( minlayer==7 )

for( i (minlayer+1) maxlayer
    if( i==2
    then
        layerlist = cons( "metal2" layerlist)
        vialist = cons( "M2_M1" vialist)
    ) ; if( i==2 )
    if( i==3
    then
        layerlist = cons( "metal3" layerlist)
        vialist = cons( "M3_M2" vialist)

```

```

) ; if( i==3 )
if( i==4
then
    layerlist = cons( "metal4" layerlist)
    vialist   = cons( "M4_M3" vialist)
) ; if( i==4 )
if( i==5
then
    layerlist = cons( "metal5" layerlist)
    vialist   = cons( "M5_M4" vialist)
) ; if( i==5 )
if( i==6
then
    layerlist = cons( "metal6" layerlist)
    vialist   = cons( "M6_M5" vialist)
) ; if( i==6 )
if( i==7
then
    layerlist = cons( "alucap" layerlist)
    vialist   = cons( "padopen" vialist)
) ; if( i==7 )
) ; for( i (minlayer+1) maxlayer )

layerlist = reverse(layerlist)
vialist   = reverse(vialist)

rectS45( cv Width Length Grid X0 Y0 layerlist vialist)

) ; pcDefinePCell

```

## Procedures to determine toroid's dimensions

```

procedure( dmin( R phi w s l )
let( (k,minDist,dist)

k=0
minDist=2*R
dist=minDist

while( ((R*sin((1+k)*phi)-R*sin(k*phi))>w && (dist>0))

dist=((1+R)*w*cos((k+0.5)*phi)-R*w*cos(k*phi)-2*l*R*sin(0.5*phi)
+(sin(phi)-2*sin(0.5*phi))*R**2-R*w*sin(k*phi)+l*w*sin((0.5
+k)*phi)+R*w*sin((0.5+k)*phi))*2/((R*cos(k*phi)-(1+R)*cos((k
+0.5)*phi))*(R*sin(k*phi)-(1+R)*sin((k+0.5)*phi))*sqrt((2
+R*sin(k*phi)-R*sin((k+1)*phi)+(w-R*cos(k*phi)+R*cos((k
+1)*phi))*((1+R)*sin((k+0.5)*phi)-R*sin(k*phi))/((1+R)*cos((k
+0.5)*phi)-R*cos(k*phi)))*2+(w-R*cos(k*phi)+R*cos((1+k)*phi)
+(R*cos(k*phi)-(1+R)*cos((k+0.5)*phi))*(w+R*sin(k*phi)-R*sin((1

```

---

```

      +k)*phi))/(R*sin(k*phi)-(1+R)*sin((k+0.5)*phi))**2))

      if( ((dist<minDist)&&(dist>0))
          minDist=dist
      ) ; if( (dist<minDist) )

      k=k+1

    ) ; while( ((R*sin((1+k)*phi)-R*sin(k*phi))>w) )

    minDist

  )
)

procedure( Rmin( w s n step )
let( (phi,R1,dist1,R2,dist2,distm)

  phi=2*Pi/n
  R1=0.5*(w+s)/sin(0.5*phi)
  dist1=dmin( R1 phi w s l )
  R2=2*R1
  dist2=dmin( R2 phi w s l )

  while( (dist2<s)
    R2=R2+R1
    dist2=dmin( R2 phi w s l )
  ) ; while( (dist2<s) )

  distm=dmin( (0.5*(R1+R2)) phi w s l )

  while( ((R2-R1)>2*step)
    if( distm>s
      then
        R2=0.5*(R1+R2)
        dist2=distm
      else
        R1=0.5*(R1+R2)
        dist1=distm
    ) ; if( distm>s )

    distm=dmin( (0.5*(R1+R2)) phi w s l )
  ) ; while( ((R2-R1)>2*step) )

  grid( R2 step )

)
)

```



## Procedures to draw the toroid

```

procedure( toro( cv n R l w step isInt mlayerlist mvialist )
let( ( i, phi;; cycle indexes
      x1, y1, x2, y2;; moving coordinates
      leff;; check for internal or external pins
      blayer, tlayer ; layers
    )

minw = 4.4
maxw = 11.99
mins = 0.6
w = max( minw grid( w 2*step ) )
w = min( maxw w )
l = max( grid( l 2*step ) (w+mins) )
if( isInt
then
  leff = 1
else
  leff = -1
) ; if( isInt )

R = max( grid( R step ) Rmin( w mins n step ) )
blayer = list()
tlayer = list()
blayer = cons( "pintext" blayer )
blayer = cons( "metal1" blayer )
tlayer = cons( "pintext" tlayer )
tlayer = cons( "metal6" tlayer )
phi=0
x1=R+0.5*(1-leff)
y1=0

for(i 0 n-1
  x2 = grid( ((R+0.5*(1+leff))*cos(phi+Pi/n)) step )
  y2 = grid( ((R+0.5*(1+leff))*sin(phi+Pi/n)) step )
  if( (y1<y2)
  then
    if( (x1<x2)
    then
      dbCreatePolygon(cv list( "metal1" "pintext" ) list( (x1-0.5*w):
        (y1-0.5*w) (x1+0.5*w):(y1-0.5*w) (x2+0.5*w):(y2-0.5*w) (x2
        +0.5*w):(y2+0.5*w) (x2-0.5*w):(y2+0.5*w) (x1-0.5*w):(y1+0.5*w)))
    else
      dbCreatePolygon(cv list( "metal1" "pintext" ) list( (x1-0.5*w):
        (y1-0.5*w) (x1+0.5*w):(y1-0.5*w) (x1+0.5*w):(y1+0.5*w) (x2
        +0.5*w):(y2+0.5*w) (x2-0.5*w):(y2+0.5*w) (x2-0.5*w):(y2-0.5*w)))
    )
  else
    if( (x1<x2)

```

```

then
    dbCreatePolygon(cv list( "metal1" "pintext" ) list( (x2-0.5*w):
        (y2-0.5*w) (x2+0.5*w):(y2-0.5*w) (x2+0.5*w):(y2+0.5*w) (x1
            +0.5*w):(y1+0.5*w) (x1-0.5*w):(y1+0.5*w) (x1-0.5*w):(y1-0.5*w)))
    else
        dbCreatePolygon(cv list( "metal1" "pintext" ) list( (x2-0.5*w):
            (y2-0.5*w) (x2+0.5*w):(y2-0.5*w) (x1+0.5*w):(y1-0.5*w) (x1
                +0.5*w):(y1+0.5*w) (x1-0.5*w):(y1+0.5*w) (x2-0.5*w):(y2+0.5*w)))
        )
    )
)

rectS( cv w w step (x2-0.5*w) (y2-0.5*w) mlayerlist
    mvialist)
phi = phi+2*Pi/n
x1 = grid( ((R+0.5*(1-leff))*cos(phi)) step )
y1 = grid( ((R+0.5*(1-leff))*sin(phi)) step )
if( (y1<y2)
then
    if( (x1<x2)
    then
        dbCreatePolygon( cv list("metal6" "pintext") list( (x1-0.5*w):
            (y1-0.5*w) (x1+0.5*w):(y1-0.5*w) (x2+0.5*w):(y2-0.5*w) (x2
                +0.5*w):(y2+0.5*w) (x2-0.5*w):(y2+0.5*w) (x1-0.5*w):(y1+0.5*w)))
        else
            dbCreatePolygon( cv list("metal6" "pintext") list( (x1-0.5*w):
                (y1-0.5*w) (x1+0.5*w):(y1-0.5*w) (x1+0.5*w):(y1+0.5*w) (x2
                    +0.5*w):(y2+0.5*w) (x2-0.5*w):(y2+0.5*w) (x2-0.5*w):(y2-0.5*w)))
            )
        )
    else
        if( (x1<x2)
        then
            dbCreatePolygon( cv list("metal6" "pintext") list( (x2-0.5*w):
                (y2-0.5*w) (x2+0.5*w):(y2-0.5*w) (x2+0.5*w):(y2+0.5*w) (x1
                    +0.5*w):(y1+0.5*w) (x1-0.5*w):(y1+0.5*w) (x1-0.5*w):(y1-0.5*w)))
            else
                dbCreatePolygon( cv list("metal6" "pintext") list( (x2-0.5*w):
                    (y2-0.5*w) (x2+0.5*w):(y2-0.5*w) (x1+0.5*w):(y1-0.5*w) (x1
                        +0.5*w):(y1+0.5*w) (x1-0.5*w):(y1+0.5*w) (x2-0.5*w):(y2+0.5*w)))
                    )
                )
            )
        )
    )

rectS( cv w w step (x1-0.5*w) (y1-0.5*w) mlayerlist
    mvialist)

) ; for(i 0 n-1)
) ; let
) ; toro

; User interface

pcDefinePCell(

```

```

list( ddGetObj( "LV_PCells" ) "toro" "layout" )

( (Width float 4.4)
  (Length float 6.4)
  (N_coils int 44)
  (Radius float 58.84)
  (Grid float 0.005)
  (Internal boolean "TRUE")
  (metal1 boolean "TRUE")
  (metal2 boolean "TRUE")
  (metal3 boolean "FALSE")
  (metal4 boolean "FALSE")
  (metal5 boolean "FALSE")
)

cv=pcCellView
blayer
mlayerlist = list( "metal1" "metal2" "metal3" "metal4"
  "metal5" )
mvialist = list( "M2_M1" "M3_M2" "M4_M3" "M5_M4" "M6_M5" )
minlayer = 6
maxlayer = 0

when( metal1 == t
  minlayer = 1
  maxlayer = 1)
when( metal2 == t
  minlayer = min( minlayer 2 )
  maxlayer = max( maxlayer 2 ))
when( metal3 == t
  minlayer = min( minlayer 3 )
  maxlayer = max( maxlayer 3 ))
when( metal4 == t
  minlayer = min( minlayer 4 )
  maxlayer = max( maxlayer 4 ))
when( metal5 == t
  minlayer = min( minlayer 5 )
  maxlayer = max( maxlayer 5 ))

if( minlayer==1
then
  mlayerlist = remd( "metal1" mlayerlist)
) ; if( minlayer==1 )
if( minlayer==2
then
  mlayerlist = remd( "metal2" mlayerlist)
) ; if( minlayer==2 )
if( minlayer==3
then
  mlayerlist = remd( "metal3" mlayerlist)
) ; if( minlayer==3 )

```

---

```

if( minlayer==4
then
    mlayerlist = remd( "metal4" mlayerlist)
) ; if( minlayer==4 )
if( minlayer==5
then
    mlayerlist = remd( "metal5" mlayerlist)
) ; if( minlayer==5 )

for( i (minlayer+1) maxlayer
    if( i==2
    then
        mlayerlist = remd( "metal2" mlayerlist)
        mvialist   = remd( "M2_M1" mvialist)
    ) ; if( i==2 )
    if( i==3
    then
        mlayerlist = remd( "metal3" mlayerlist)
        mvialist   = remd( "M3_M2" mvialist)
    ) ; if( i==3 )
    if( i==4
    then
        mlayerlist = remd( "metal4" mlayerlist)
        mvialist   = remd( "M4_M3" mvialist)
    ) ; if( i==4 )
    if( i==5
    then
        mlayerlist = remd( "metal5" mlayerlist)
        mvialist   = remd( "M5_M4" mvialist)
    ) ; if( i==5 )
) ; for( i (minlayer+1) maxlayer )

mlayerlist = reverse(mlayerlist)
mvialist   = reverse(mvialist)

toro( cv N_coils Radius Length Width Grid
      Internal mlayerlist mvialist)

) ; pcDefinePCell

```



## APPENDIX E

# Publications

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The following papers resulted from the different research projects related to this study.

## Published

- Andreani, P., Wang, X., Vandi, L. and Fard, A., “A Study of Phase Noise in Colpitts and LC-Tank CMOS Oscillators”, *IEEE Journal of Solid-State Circuits*, vol. 40, no. 6, 2005. [\[94\]](#)
- Vandi, L., Andreani, P., Temporiti, E., Sacchi, E., Bietti, I., Ghezzi, C. and Castello, R., “Toroidal inductors in CMOS processes”, *Proceedings of IEEE 23<sup>rd</sup> NORCHIP Conference*, 2005. [\[82\]](#)
- Liscidini, A., Mazzanti, A., Tonietto, R., Vandi, L., Andreani, P. and Castello, R., “A 5.4mW GPS CMOS Quadrature Front-End Based on a Single-Stage LNA-Mixer-VCO”, *Proceedings of IEEE International Solid-State Circuits Conference*, 2006. [\[1\]](#)

## Accepted for publication

- Vandi, L., Andreani, P., Temporiti, E., Sacchi, E., Bietti, I., Ghezzi, C. and Castello, R., “A toroidal inductor integrated in a standard CMOS process”, Accepted for publication on *Springer Analog Integrated Circuits and Signal Processing International Journal*. [95]
- Liscidini, A., Mazzanti, A., Tonietto, R., Vandi, L., Andreani, P. and Castello, R., “Single-Stage Low Power Quadrature RF Receiver Front-End: The LMV cell”, Accepted for publication on *IEEE Journal of Solid-State Circuits*. [66]

## Submitted for publication

- Vandi, L., Andreani, P., Tired, T. and Mattisson, S., “A novel approach to negative feedback in RX front-ends”, Submitted for publication to *IEEE 24<sup>th</sup> NORCHIP Conference*, 2006. [96]

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